HP 7979A/S, 7980A/S, 7980XC/SX, 88780A/B

Service Manual

HEWLETT
PACKARD

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Notice

FCC Radio Frequency Interference Statement

(USA Only) This equipment generates and uses radio frequency energy and, if not installed and used properly (that is, in strict accordance with the manufacturer's instructions) may cause interference to radio and television reception. The equipment has been type tested and found to comply within the limits for a Class A computing device in accordance with the specifications in Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference in a commercial environment. Operation of this equipment in a residential area is likely to cause interference.

If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Re-orient the receiving antenna.
- Relocate the computer equipment with respect to the receiver.
- Move the computer away from the receiver.
- Plug the computer into a different outlet so that computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions.

The Federal Communications Commission has prepared a booklet entitled *How to Identify and Resolve Radio - TV Interference Problems* which may be helpful to you. This booklet (stock #004-000-00345-4) may be purchased from the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402.

United Kingdom Telecommunications Act 1984

The HP 7979A/S, 7980A/S, 7980SX/XC, and 88780A/B Tape Drives are approved under Approval Number NS/G/1234/J/100003 for indirect connection to Public Telecommunication Systems within the United Kingdom.

Funkentstörung Deutschland

Herstellerbescheinigung

Hiermit wird bescheinigt, daß die Gerät HP 7979A/S, 7980A/S, 7980SX/XC, and 88780A/B in Übereinstimmung mit den Bestimmungen von Postverfügung 1046/84 funkentstört ist. Der Deutschen Bundespost wurde das Inverkehrbringen dieses Geräte angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

Wird das Gerät innerhalb einer Anlage betrieben,

- so muß bei Inanspruchnahme der Allgemeinen Genehmigung FTZ 1046/84 die gesamte Anlage der oben genannten Genehmigung entsprechen.

- die mit einer FTZ-Serienprüfnummer gekennzeichnet ist, und für die eine Betriebsgenehmigung vorliegt oder beantragt wird, so sind in der Regel keine weiteren Schritte notwendig.

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従って，住宅地域またはその隣接した地域で使用すると，ラジオ，テレビジョン受信機等に受信障害を与えることがあります。

取扱説明書に従って正しい取り扱いをして下さい。

Printing History

New editions of this manual incorporate all material updated since the previous edition. The manual printing date and part number indicate its current edition. The printing date changes when a new edition is printed. (Minor corrections and updates incorporated at reprint do not cause this date to change.)

Edition 1 .... May, 1987

Edition 2 .... January, 1988

Edition 3 .... July, 1989

Edition 4 .... October, 1991

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Product Information

1.1 Product Features

The HP 7979A/S, 7980A/S, and 7980XC/SX are autoloading, horizontally rack-mounted, 1/2-inch reel-to-reel tape drives. The HP 88780A/B is the OEM/Distributor version of the HP 7980 with a SCSI or Pertec-Compatible Interface and Data Compression options.

These drives offer the following features:

- Low cost
- Compact, ergonomic design
- Front autoload
- Simplified control panel
- Versatile handling of all standard-sized reels (6 to 10 1/2-inch)
- 125 ips nominal tape speed for maximum streaming performance
- Density configuration as needed: the 7979A/S supports 1600 cpi PE recording, the 7980A/S, 7980XC/SX, and 88780A/B support both 1600 cpi and 6250 cpi GCR recording. The Option 800 supports 800 cpi NRZI recording on the 7979A/S, 7980A/S, and 88780A/B. Option 800 is not available on the 7980XC/SX.
- Large cache buffer for fast transfers during start-stop applications; 512 Kbyte or 1 Mbyte. All current products except those with data compression are shipped with 1 Mbyte cache buffer.
- Extra capacity data compression data storage at 6250 cpi selectable by operator or through host on 7980XC and 7980SX; data storage per tape increased by two to five times.
- Easy to use diagnostics

- Custom operating features, selected from the control panel or through the host computer.
- Standard 19-inch EIA rack mount
- HP-IB interface available for the 7979A, 7980A, and 7980XC. Single-ended HP Common SCSI (HPCS) available for the 7979S, 7980S, 7980SX.

  The 88780A/B may be equipped with the Pertec-compatible interface or the Small Computer System Interface (SCSI) in either single or double-ended configurations.
- Low power consumption

1.2 Specifications

Table 1-1. Drive Specifications

Performance Characteristics	7979A/S	7980A/S 88780A/B	7980XC/SX 88780 Opt 400
Burst Transfer Rate (max.)[1]			
6250XC	N/A	N/A	1000 Kbytes/s
6250 GCR	N/A	769 Kbytes/s	769 Kbytes/s
1600 PE	208 Kbytes/s	208 Kbytes/s	208 Kbytes/s
800 NRZI	104 Kbytes/s	104 Kbytes/s	N/A
Transfer Rate to Tape (avg.)			
6250 GCR	N/A	747 Kbytes/s	747 Kbytes/s
		(64K blocks - 0.3-inch gap)	
1600 PE	198 Kbytes/s	198 Kbytes/s	198 Kbytes/s
		(16K blocks - 0.5-inch gap)	
800 NRZI	99 Kbytes/s	99 Kbytes/s	N/A
	(8K blocks - 0.5-inch gap)		
Speed(nominal)			
Read/Write			
GCR		123 ips	123 ips
PE/NRZI	130 ips	130 ips	130 ips
Rewind		320 ips avg., 450 ips max.	
		(90 seconds to rewind a 2400-ft tape)	

1 These rates are the maximum tape drive potential and do not reflect actual transfer rates, which depend on the host used.

Table 1-1. Drive Specifications (continued)

Performance Characteristics	7979A/S	7980A/S 88780A/B	7980XC/SX 88780 Opt 400
Density			6250XC
			(Compressed)
		6250 cpi	6250 cpi
	1600 cpi	1600 cpi	1600 cpi
	800 cpi (Opt.800)	800 cpi (Opt.800)	
Formatted Data Capacity			
(2400-ft reel)			
	40 Mbytes	140 Mbytes	200-700 Mbytes
	(typ. 1600 cpi)	(typ. 6250 cpi)	
		40 Mbytes	
		(typ. 1600 cpi)	
	20 Mbytes	20 Mbytes	
	(typ. 800 cpi)	(typ. 800 cpi)	
Max. Block Size on Tape[1]			
6250 GCR	N/A	256 Kbytes	256 Kbytes
1600 PE	64 Kbytes	64 Kbytes	64 Kbytes
800 NRZI	64 Kbytes	64 Kbytes	N/A

[1]Block may be limited by host operating system.

Table 1-2. Reliability

Tape Drive	Data Compression	GCR	PE	NRZI
7979A/S				
Read	N/A	N/A	1 in 10^{10}	1 in 10^{10}
Write	N/A	N/A	1 in 10^{09}	1 in 10^{09}
7980A/S, 88780A/B				
Read	N/A	1 in 10^{11}	1 in 10^{10}	1 in 10^{10}
Write	N/A	1 in 10^{10}	1 in 10^{09}	1 in 10^{09}
7980XC/SX				
Read	1 in 10^{11}[1]	1 in 10^{11}	1 in 10^{10}	N/A
Write	1 in 10^{10}	1 in 10^{10}	1 in 10^{9}	N/A
MTBF	30,000 hours			

1 Because less tape is written per amount of data, the number of bytes stored per error is less than 1 in 10^{11}. However, if a record is unreadable it would represent more data than with industry-standard 6250 cpi density.

Table 1-3. Functional Characteristics

Tape Drive	Interface Options	Internal Buffer Size	Operating Mode
HP7979A/7980A/7980XC	HP-IB (IEEE 488)	512K or 1Mbyte	Streaming
HP7979S/7980S/7980SX	HPCS (HP Common SCSI, Single Ended)	1 Mbyte	Streaming
HP88780A/B	Pertec-Compatible SCSI Single-ended SCSI Differential	512K or 1 Mbyte	Streaming

Table 1-4. Power Requirements

Line Voltage (±10%)	90-125 VAC 198-250 VAC
Line Frequency	50-60 Hz
Power Consumption	
Maximum	250 Watts
Standby	20 Watts
Idle	170 Watts

Table 1-5. Physical Specifications

Tape Drive w/o Rack	
	HP 7979A/S;7980A/S;7980XC/SX;88780A/B
Height	222 mm (8.75 in.)
Width	483 mm (19.0 in.)
Depth	673 mm (26.5 in.)
Weight	38.5 kg (85 lbs)
	HP 88780B - 31.0 kg (68 lbs)
Tape Drive In The Rack	
	HP 7979A/S;7980A/S;7980XC/SX
Height	1000 mm (39.37 in.)
Width	600 mm (23.62 in.)
Depth	800 mm (31.5 in.)
Weight	136.5 kg (300 lbs)
Shipping Weight	177.25 kg (390 lbs)

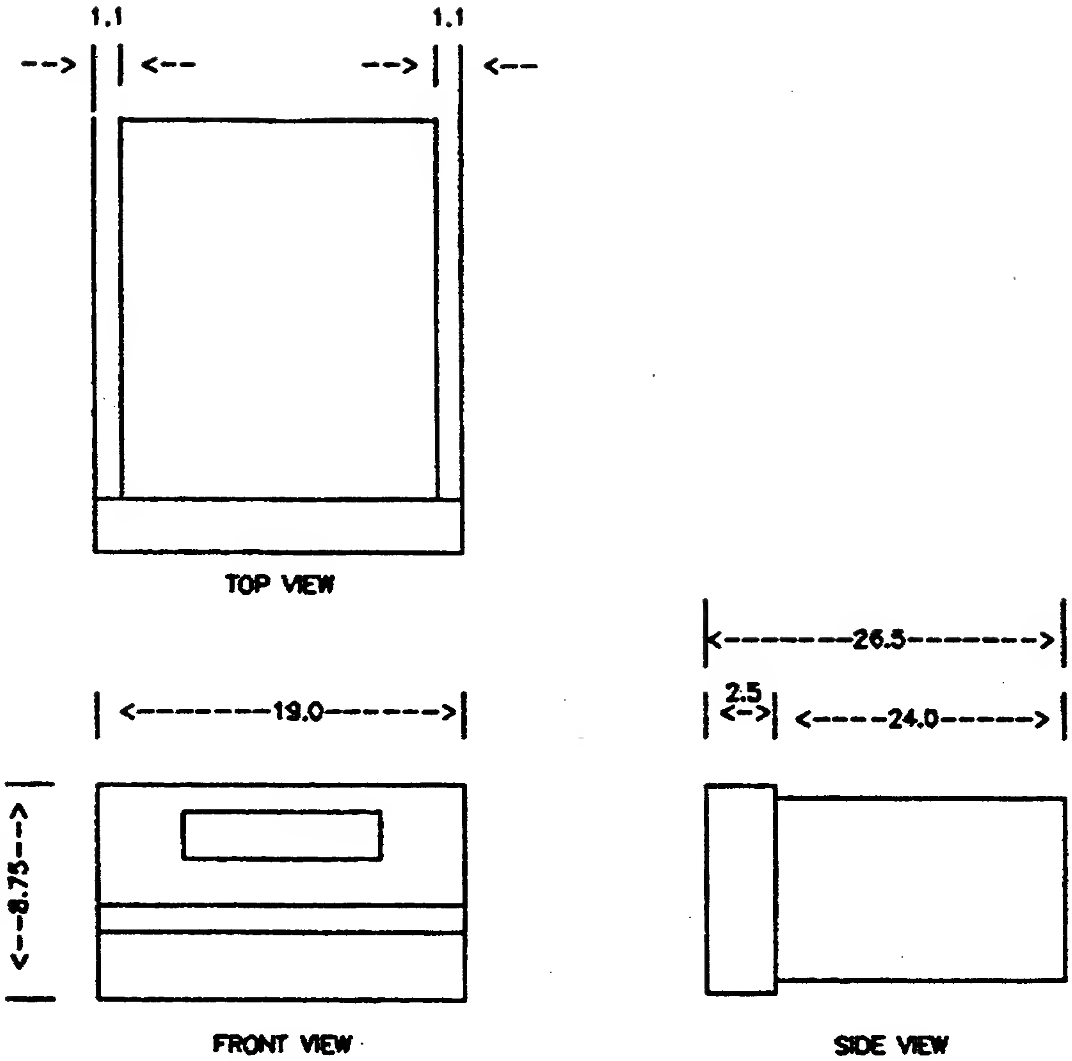

Figure 1-1. Drive Dimensions (in inches).

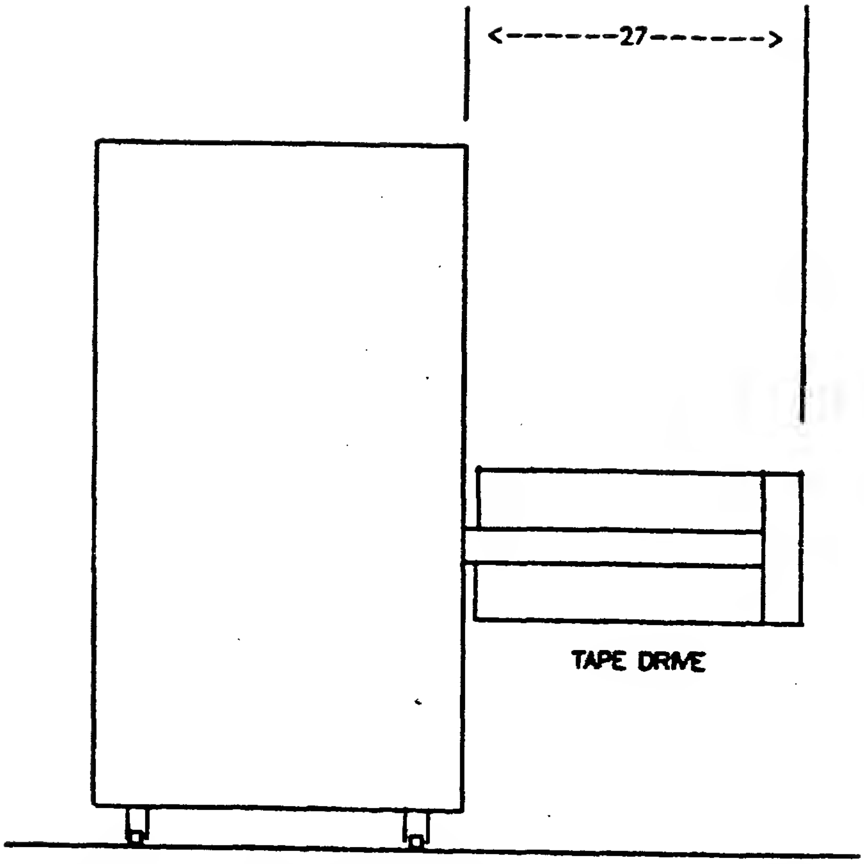

Figure 1-2. Drive in Standard EIA Rack (side view)

Table 1-6. Tape Specifications

	HP 7979A/S;7980A/S;7980XC/SX;88780A/B
Width	12.7 mm (0.5 in.)
Thickness*	0.038 mm (1.5 mils)
	Tape should meet or exceed ANSI X3.40-1983)
*see "Using 1-Mil Tape" after these tape specifications.	
Tension	283 g
	(10 oz ±1 oz)
Reel Sizes	267 mm (10.5 in.)
	216 mm (8.5 in.)
	178 mm (7.0 in.)
	152 mm (6.0 in.)

Using 1-MIL Tape

The following statement appears in the *HP 7979A/S/7980A/S/7980XC/SX Tape Drive User's Guide* and the *HP 88780A (now "B") Tape Drive User's Guide*.

Hewlett-Packard supports the use of 1-mil (3600-ft reel) tapes on the 1/2- inch tape drives under certain conditions. These conditions are stated at the end of the following background information.

Electrically and magnetically, 1-mil tapes are equivalent to ANSI-standard 1.5-mil mil tapes, but do not meet ANSI thickness specifications due to their thinner Mylar substrate. **Thin tape was designed for low-speed datalogging operations.**

Two characteristics of 1-mil tape must be taken into account before this tape is used; 1-mil tapes are more susceptible to deformation and breaking, and thin tapes conform to the read/write heads differently and therefore wear the heads differently than 1.5-mil tapes.

With regard to tape deformation, the 1/2-inch tape drives will physically handle 1-mil tapes without deforming or breaking them. All tape operations

are supported, including autoload. However, drive cleaning is critical when using 1 mil tapes. Because of susceptibility to deformation, 1 mil tapes can be destroyed in a single pass on a dirty tape drive.

Note Some tape manufacturers recommend use of 1.5 mil leader material when their tapes are used in autoload drives. Manufacturer's recommendation should be followed.

With regard to different head wear patterns, the 1/2-inch tape drive heads are affected by use of 1-mil tape in the same way as heads on any other tape drive; the critical read/write area of the head wears at an increased rate and forms a different profile from that made by 1.5-mil tape.

When a 1.5-mil tape is mounted on a drive in which the read/write area of the head has been worn by frequent use of 1-mil tape, the thicker 1.5-mil tape cannot conform to the wear profile caused by the 1-mil tape and will pass over the read/write area of the head at a greater distance. This increased tape-to-head distance causes signal loss. The effect of signal loss can be an increase in read and write errors. This effect is true for all industry-standard half-inch tape drives.

Because of the incompatibility of the head wear profiles, Hewlett-Packard can support the use of 1-mil tapes on the 1/2-inch tape drives only if the following guidelines are used:

- if a significant portion (more than 1 tape in 10) of the tapes used on the drive are 1-mil tapes, we recommend that a drive be dedicated to the use of the thinner tapes.
- if less than 1 tape in 10 used on the drive is a 1-mil tape, AND at least 10 1.5-mil tapes are mounted between the mountings of the 1-mil tapes, the two tape types can be used on the same drive.

Table 1-7. Environmental Specifications

	HP7979A/S, 7980A/S 7980XC/SX, 88780A/B
Temperature	
Operating	15-32° C (limited by media)
Non-Operating	0-55° C
Storage	-40° to 70° C
Rate of Change	20° C per hour
Relative Humidity	
Operating	Tape medium limited to 20%-80% at <20° C maximum wet bulb temperature
Storage/Shipment	Tape medium limited to 90% at 40° C maximum wet bulb temperature
Altitude	
Operating	3000 m (10,000 ft)
Non-Operating	15,300 m (50,000 ft)
Shock	
Transportation	Trapezoidal pulse, 188 ips, 30 g
End-Use	Half-sine pulse, 57 ips, 3ms duration
Vibration	
Operating Random	
(~0.21 g RMS)	5-500 Hz
Non-Operating Random	
(~2 g RMS)	5-500 Hz
Non-Operating Swept Sine	
(0.5 g peak)	5-500 Hz

Table 1-7. Environmental Specifications (continued)

	HP7979A/S, 7980A/S 7980XC/SX, 88780A/B
Audible Noise	
(weighted sound power)	
Read Write Operation	6.6 Bels (A)
Tape Loading Operation	7.2 Bels (A)
Heat Dissipation	1280 BTU/hr maximum

Particulates

The suspended particulate count should not be greater than 55 micrograms per cubic meter (per CSD guidelines for EDP environment).

ESD Considerations

The HP 7979A/S; 7980A/S/XC/SX; 88780A/B can withstand a 5 Kv discharge without any perceived errors, and a 15 Kv discharge without a permanent hardware error or causing a system reset or loss of data.

Cooling Requirements

A minimum of 70 to 80 mm (3 in.) is required behind the rear door to allow for air circulation. Maintain a clearance of at least 1 meter (39 in.) in front of the cabinet for opening the front door and for pulling the unit out during servicing.

1.3 Regulatory Approval

Safety

Underwriters Laboratories

UL 478, 5th Edition (UL listed)

Canadian Standards Association

C22.2 No. 220-M1986 (CSA certified)

International Electrotechnical Commission

IEC 380, 435 (complies) Newer 88780B units meet IEC 950

Technischer Uberwachungs-Verein Bayern Inc. (TUV certified)

HP7979A/S; 7980A/S; 7980XC/SX	- DIN IEC 380/VDE 0806/08.81
HP88780A/B	- DIN VDE 0805/05.90 EN 60950

1.4 Options

HP-Connect Products

HP 7979A/S - 1600 cpi autoload drive with 512 Kbytes or 1 Mbyte Data Buffer and 1 meter cabinet. Includes interface cable, accessories and installation. 1 Mbyte Data Buffer shipped with all current 7979A/S products.

To order two drives in one cabinet, order one 7979A/S Option 100 plus one 7979A/S Option 133.

HP 7980A/S - 1600/6250 cpi autoload drive with 512 Kbytes or 1 Mbyte Data Buffer and 1 meter cabinet. Includes HP-IB cable, accessories and installation. 1 Mbyte Data Buffer shipped with all current 7979A/S products.

To order two drives in one cabinet, order one 7980A/S Option 100 plus one 7980A/S Option 133.

HP 7980XC/SX -	1600/6250/6250XC cpi Extra Capacity autoload drive with 512 KB Data Buffer and 1 meter cabinet. Includes HP-IB cable, accessories and installation.
	To order two drives in one cabinet, order one 7980XC/SX Option 100 plus one 7980XC/SX Option 133.
	All drives must be ordered with one of the following cabinet or drive mounting options:
Option 100 -	Includes drive mounted in 1-meter cabinet, standard front door, bezel shroud. *Price includes installation.*
Option 133 -	Add-on drive. Includes drive, short lower panel, bezel shroud, standard slide rails. *Price includes installation.*
Option 135 -	Drive Only (installation in another 19-inch rack). Includes drive only. *Price DOES NOT include installation.*
Option 137 -	Preparation for addition of disc drive. Includes drive mounted in 1-meter cabinet, door with window, bezel shroud. *Price includes installation (tape drive only).*
	Order when installing an HP 7976/37 disc drive in the bottom of the tape drive cabinet. The HP 19512A Disc Drive Rackmount Kit should be ordered separately from DMD.
Option 1A4 -	Preparation for installation in HP A1001A (1.6 meter) cabinet. Includes drive, special slide rails. *Price includes installation.*
	All drives must be ordered with one of the following density options:
Option 200 -	Does not read or write 800 cpi (NRZI). This was the former "standard" drive.
Option 800 -	Will read and write 800 cpi (NRZI). This option is not available with the 7980XC or 7980SX.

Upgrade paths

HP 88703A - HP 7979A/S to HP 7980A/S. Includes on-site installation by HP. Not customer installable.*

HP 88705A - HP 7980A/S to HP 7980XC/SX. Includes on-site installation by HP. Not customer installable.*

*An HP 7979A/S may be upgraded to an HP 7980XC/SX by installing both the HP 88703A and the HP 88705A.

HP 88707S #079 - This kit converts the 7979A to a 7979S. It replaces the firmware, Buffer PCA, HP-IB interface, display window, and rear door of the 1-meter rack. Includes on-site installation by HP. *Not customer installable.*

HP 88707S #080 - This kit converts the 7980A to a 7980S. It replaces the firmware, Buffer PCA, HP-IB interface, display window, and rear door of the 1-meter rack. Includes on-site installation by HP. *Not customer installable.*

HP 88707S #081 - This kit converts the 7980XC to a 7980SX. It replaces the firmware, HP-IB interface, display window, and rear door of the 1-meter rack. Includes on-site installation by HP. *Not customer installable.*

Note

A customer can trade-in the HP-IB interface when purchasing the HP 88707S kit and receive a credit (Order Option 100). When Option 100 is ordered, the HP-IB PCA and the Buffer PCA (if included) must be returned to HP SMO using the prepaid mailing labels included in the upgrade kit. This upgrade kit will be made available to customers who want to move their HP-IB tape drives over to SCSI. There **will not** be a trade-in credit for trading in an OEM SCSI interface for a HP-connect SCSI interface.

HP 88780A/B (Distributor Models)

HP 88780B - (new orders for "A" model discontinued) 1600/6250 cpi autoload drive with 512 KB or 1 MB Data Buffer.

Interface, accessories, mounting hardware, and cabinet are not included. An order must include interface selection. Not intended for HP computer systems.

Order an interface by specifying Option 007 plus the Interface Kit desired (HP 88753A, 88754A, or 88755A).

Option 007 -	Interface Preparation Provides both SCSI and Pertec-compatible interface firmware. The applicable firmware is mounted on the PCA included in the Interface Kit ordered with the drive (HP 88752A, 88754A, or 88755A).
Option 131 -	Desktop Enclosure for HP 88780A Standalone cabinet for tape drive. Designed for desktop use. If ordered as an add-on, order HP 88706A described below.
Option 132 -	Desktop Enclosure for HP 88780B Standalone cabinet for tape drive. Designed for desktop use.
Option 142 -	Rotating Rack Slides for the HP 88780B Rack slides for mounting in a 19-inch rack enclosure. If ordered as an add-on, order HP 88709A Rotating Rack Slide Kit.
Option 400 -	Data Compression (only supported on SCSI drives) Adds data compression. Formats available are 1600 PE, 6250 GCR and 6250 XC (Extra Capacity.)
Option 800 -	800 cpi NRZI Adds 800 cpi density Non-Return to Zero Inverted (NRZI) format. Not offered in kit form. Must be ordered with the drive.
HP 88752A Kit -	Pertec-compatible Interface Kit

Pertec-compatible interface. Includes pertec-compatible interface PCA and mounting hardware. Cables not included.

HP 88754A Kit - Single-Ended SCSI Kit

Single-Ended Small Computer Systems Interface (SCSI) Kit. Includes Single-Ended SCSI Interface PCA and mounting hardware. Cables not included.

HP 88755A Kit - Differential SCSI Kit

Differential Small Computer Systems Interface (SCSI) Kit. Includes Differential SCSI Interface PCA and mounting hardware. Cables not included.

HP 88706A Kit - Desktop Enclosure

Standalone cabinet. Designed for using the HP 88780A/B on a desktop.

HP 88709A Kit - Rack Slide Kit

Rotating Rack Slide Kit for the HP 88780A/B.

The following interface options *were* available (before July 1989) on the HP 88780A (given here for information only). These options are not orderable on the HP 88780B.

Option 002 - (Pertec-compatible Interface)

Added Pertec-compatible interface PCA. Cables not included.

Option 004 - SCSI Single-Ended Interface

Added single-ended version of Small Computer Systems Interface (SCSI) PCA. Cables not included.

Option 005 - SCSI Differential Interface

Added differential-ended version of Small Computer Systems Interface (SCSI) PCA. Cables not included.

1.5 Accessories

Table 1-8. Accessories

Description	Customer Order Number	HP Number
Magnetic Tape, 1200-ft (box of 10)	92150E	
Magnetic Tape, 2400-ft (box of 10)	92150F	
Lint-free Wipes (bag of 100)	92193W	
Magnetic Tape Sense (BOT/EOT) Markers (card of 250)	92150M	
Isoprophyl Alcohol from DMK	92281B	
Foam Swabs (package of 50)		9300-0767
Foam Swabs (package of 50)		9300-0468

2

Site Preparation / Requirements

2.1 Site Preparation

The following paragraphs discuss the requirements for proper operation of the tape drive. For detailed site environmental information, refer to the publication entitled *Site Environmental Requirements for Tape Drives* HP Part No 5955-3456.

2.2 Environmental Requirements

The tape drive is designed to operate with an ambient air temperature range of 15° to 32° C (60° to 90° F) with a rate of temperature change not to exceed 20° C (36° F) per hour. See *Cooling Requirements* for the recommended operating range.

Note

The environmental specifications listed here apply when the tape drive is not connected to a Hewlett-Packard system. When this device is connected to HP systems, the more stringent environmental specifications listed for any single HP device within the HP system are applicable and supersede these specifications.

2.3 Primary Power/External Ground

The female power outlet to be used to supply AC power to the tape drive must be checked by a certified electrician to ensure that the proper voltage is available for the tape drive. Permitted voltage range(s), depending on configuration and assuming 48-66 Hz, are 90 to 125 VAC (120 VAC nominal) and 198 to 250 VAC (220 VAC nominal). Also check the earth (safety) ground in the power outlet.

Be aware that the electrical load imposed by the tape drive may reduce the available voltage below the non-load value. If the line voltage, when loaded, is not within the correct range, check for proper wiring.

2.4 Cooling Requirements

A minimum of 70-80 mm (3 in.) is required behind the rear door of the cabinet to allow air circulation. Maintain a clearance of at least 1 meter (39.37 in.) in front of the cabinet to provide adequate space for opening the front door (490 mm / 19.3 in.) and for pulling the unit out during servicing.

The area does not have to be air-conditioned, but maintaining an operating room temperature between 18° C to 24° C (65° F to 75° F, non-condensing) is RECOMMENDED.

2.5 Location Requirements

Position the drive away from sources of particulate contamination such as frequently-used doors and walkways, stacks of supplies that collect dust, and smoke-filled rooms. If possible, allow enough room at the rear of the cabinet for access to the power switch (inside the rear cabinet door) and for service.

3

Installation and Configuration

Note

The HP 88780A/B is basically an HP 7980A/S sold to distributors or modified to OEM requirements. These requirements, and therefore the operation and physical appearance of the drive, may vary from OEM to OEM.

Installation of an HP 88780A/B may be by the OEM; and some general procedures described here may not be applicable to a specific OEM drive.

With this in mind, the installation procedures described in this chapter include the HP 88780A/B as if it were being installed by Hewlett-Packard service personnel. These procedures are included only as a general aid to OEMs that choose to use this Hewlett-Packard manual as their product reference. The OEM should evaluate these procedures and modify them as necessary.

The following setup steps and operation information are described in this chapter:

- Setting the tape drive voltage
- Connecting the tape drive to the host system using a(n)
  - HP-IB Interface
  - SCSI Interface
  - Pertec-Compatible Interface
- Reseating all PCAs
- Connecting the power cable and switching on the tape drive
- Clearing the drive's non-volatile RAM (NVRAM)
- Computing the autogain values
- Setting the tape drive Address/ID number
- Storing the configurations to tape
- Operating the Tape Drive
  - Using the control panel
  - Loading a tape
  - Unloading a tape
- Control panel display messages

3.1 Setting the Voltage

1. Remove power from the tape drive by doing the following:
   a. Toggle the front panel **Standby Switch** to the out (OFF) position.
   b. Press the "0" side on the **Main AC Power Switch** on the rear panel to remove power from the drive.
   c. Disconnect the power cable.
2. Set the voltage configuration by doing the following:
   a. Slide the fuse module out.

   The fuse module is located directly under the power cable receptacle on the rear of the drive unit. When the power cable is removed, a small slot on the top of the module can be accessed. Insert your fingernail or a small screwdriver into this slot to help slide the module out from its flush-mounted position. Pull the fuse module all the way out.

Warning

The correct fuse for the selected voltage must be in the proper receptacle in the holder.

Operation	Fuse	HP Part Number
120 volt (115 VAC nominal)	6 A 250 V	2110-0056
220 volt (220 VAC nominal)	3 A 250 V	2110-0655

Viewed from the end of the fuse holder as the holder is being inserted, the "active" fuse will be on the right side of the holder—the same side as the Voltage Reference Mark.

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   b. Rotate the fuse module so that the desired voltage rating arrow ("110 -120 V" or "220 - 240 V") aligns with the arrow on the lower edge of the receptacle. Ensure that the correct fuse is in on the right side (see WARNING).

c. Replace the fuse module.

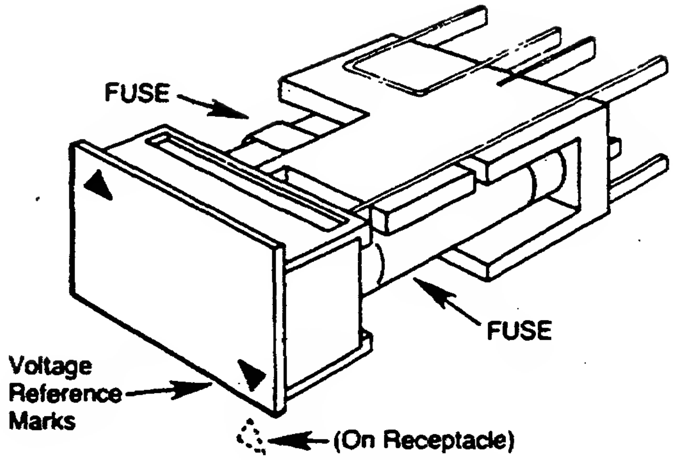

Figure 3-1. Fuse Module

3.2 Connecting to the Host

This section is divided into three procedures:

- Connecting with an HP-IB Interface
- Connecting with a SCSI Interface
- Connecting with a Pertec-Compatible Interface

General Steps

1. Locate the appropriate host interface cable.
2. Connect the host interface cable to the Interface Connector located on the rear of the drive unit.
3. Connect the host interface cable to the host system CPU.

Connecting with an HP-IB Interface

- Make sure power is off to the drive.

  The front panel Standby Switch is in the out (OFF) position.
  The Main AC Power Switch on the rear panel is in the "0" position.

- Disconnect the power cable from the rear of the drive.
- Determine the proper HP-IB loading from the cabling situation.

  HP-IB cabling requires that the total cable lengths ("loads") in a configuration, both internal and external, must not exceed the total cable lengths supported by the devices in that configuration. Cable lengths are expressed in meters.

  The maximum allowed length of the HP-IB cable which connects devices to a General I/O Channel (GIC) is seven meters plus one meter for each device (most devices, including the 1/2-inch tape drives, support a load of one meter—unless you change the loading in the 7979A/S, 7980A/S, or 7980XC/SX).

  Two meters are used internally in the System Processor Unit (SPU) and must be subtracted from the total cable allowed. This leaves five meters plus one meter for each device—the total cable supported then becomes six.

The cable length between the 7979A/S/7980A/S/7980XC/SX drive HP-IB Interface PCA and the rear panel of the cabinet

- is included in the HP-IB PCA transceiver loading,
- does not count as an external cable length,
- and is not subtracted from the one external load supported by the drive.

The following example shows both the internal and external cable length loads of a simple system and shows how to calculate the maximum amount of cable allowed between the GIC and the tape drive. The example assumes a HP3000 Series 64 computer using a GIC supporting seven meters of cable with two meters of cable internally (from the SPU to the outside of the cabinet).

Example: Determining HP-IB Cable Load

External Cable Length	
GIC to I/O Panel	+ 1 m
I/O Panel to Tape Drive	+ 7 m
Internal Cable Length	
Inside tape drive	- 0 m
Inside GIC	- 2 m
Cable Available	+ 6 m

When all supported external cable lengths (pluses (+) in this case) are added to all existing internal cable lengths (minuses in this case), the optimum result should be zero. If there is a difference, it must be on the side of HAVING MORE CABLE SUPPORTED than actually used. Loads must be balanced between each peripheral as they are added to the HP-IB loop. Trying to balance the whole HP-IB loop by placing loads in the last peripheral will not work.

If more cable length is used than is supported by the combination of GIC and peripherals, spurious and hard-to-find errors will most probably be introduced into the system.

Note

Short HP-IB cables should not be linked together to make a longer cable. Use a single cable of the correct length.

A GIC supports from 1 to 8 HP-IB peripherals. Depending on the type of peripheral and its time of use, connecting other peripherals to the GIC that supports this drive might degrade the performance of the drive to an unacceptable level.

- Install loading resistor packs, as needed, on the HP-IB Interface PCA using the following diagram as a guide.

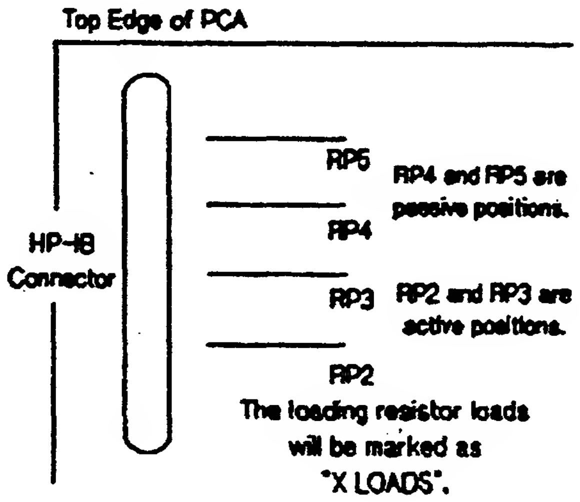

Figure 3-2. HP-IB Load Resistors

Connecting with a SCSI Interface

The SCSI Bus must be resistively terminated at both ends. Typically, one end is terminated by the computer, the other end is, in the case of these HP tape drives, terminated by an external terminator inserted into an unused cable connector on the interface PCA (if the drive is the last device on the Bus).

To make the termination work, the termination must be supplied with +5 V. This voltage is called Termpower.

On the SCSI Interface PCAs, selecting the source of the Termpower is done by the JM2 jumper. The two positions available are:

- "Initiator Termpower"—the host computer supplies the power
- "Device Termpower"—the peripheral device supplies the power.

The default setting is "Initiator Termpower."

Distribution Of Termpower (Single-Ended SCSI Interface PCA)

If 88780-6xx15 PCA: The distribution of Termpower on the Single-Ended SCSI Interface. PCA (-6xx15) depends on the configuration of the R1 jumper wire. This wire is located between the jumper JM2 and the large, square IC—close to the top edge of the PCA.

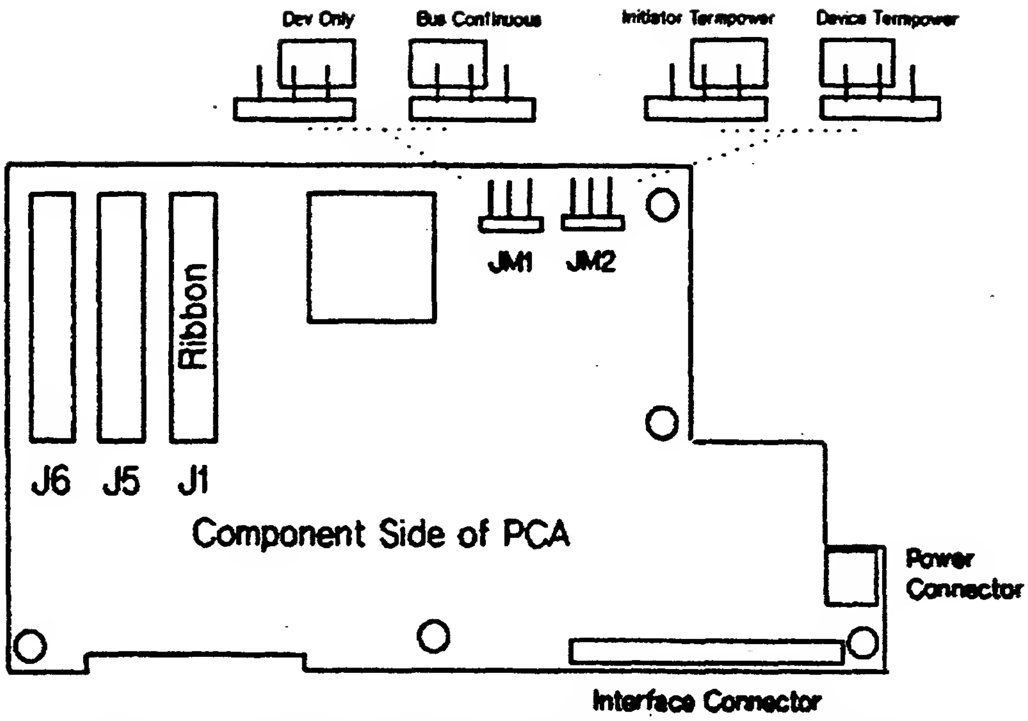

Figure 3-3. Single-Ended SCSI Interface (88780-6xx15)

There are three possibilities.

- If "Initiator Termpower" is selected on JM2, the configuration of R1 does not matter. Drive interface does not supply any Termpower.
- If "Device Termpower" is selected on JM2 and R1 is in place, Termpower is supplied to all three SCSI connectors.
- If "Device Termpower" is selected on JM2 and R1 is removed (cut), Termpower is supplied only to the J6 SCSI connector.

There is diode protection on the +5 V line for protection when more than one device supplies power to the SCSI Bus.

Caution If the host computer GROUNDs Termpower and the tape drive is supplying Termpower, the interface supply will be grounded and the interface fuse will blow.

If 88780-6xx35 PCA: The distribution of Termpower on the Single-Ended SCSI Interface. PCA (-6xx35) depends on the configuration of the JM1 jumper. This jumper is located between the jumper JM2 and the large, square IC—close to the top edge of the PCA.

There are three possibilities.

- If "Initiator Termpower" is selected on JM2, the position of JM1 does not matter. Drive interface does not supply any Termpower.
- If "Device Termpower" is selected on JM2 and JM1 is set to "Bus Continuous", Termpower is supplied to all three SCSI connectors.
- If "Device Termpower" is selected on JM2 and JM1 is set to "Dev Only", Termpower is supplied only to the J6 SCSI connector.

There is diode protection on the +5 V line for protection when more than one device supplies power to the SCSI Bus.

Caution If the host computer GROUNDs Termpower and the tape drive is supplying Termpower, the interface supply will be grounded and the interface fuse will blow.

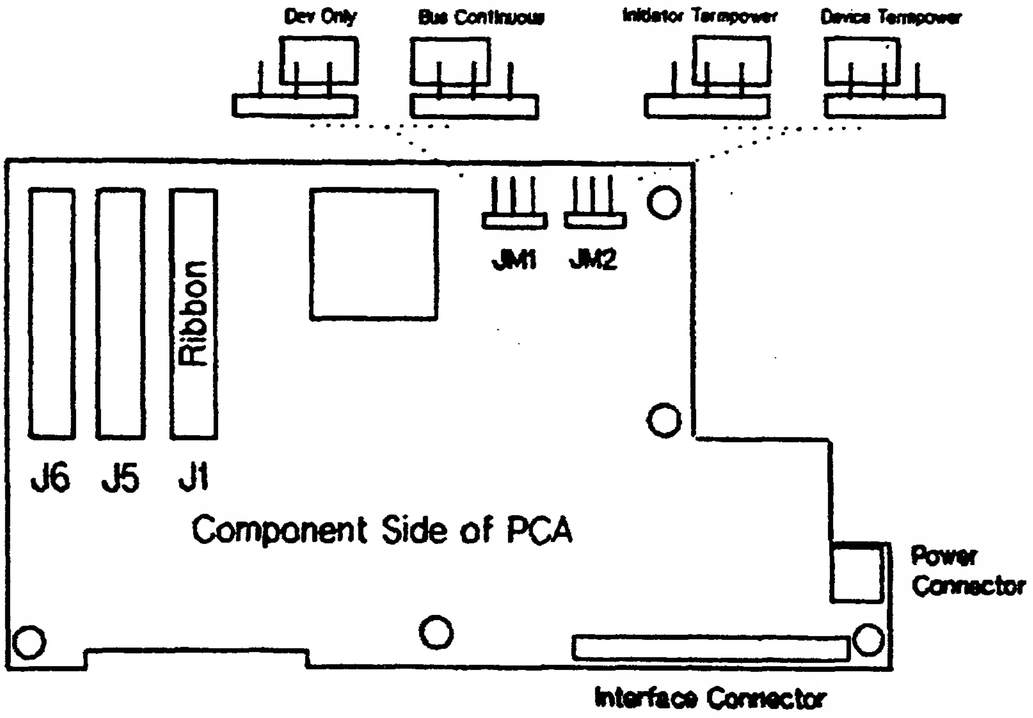

Figure 3-4. Single-Ended SCSI Interface (88780-6xx35)

Distribution Of Termpower (Differential SCSI Interface PCA)

If 88780-6xx16 & 88780-6xx36:. The selection of the "Initiator" or "Device" supply for Termpower using JM2 is the same as on the Single-Ended SCSI Interface. If "Device Termpower" is selected, Termpower is supplied to both SCSI connectors on the PCA.

Connecting with a Pertec-Compatible Interface

The Pertec-compatible Bus must be terminated at both ends. Typically, one end is terminated at the computer and the other end, in the case of these HP tape drives, is terminated by Termination Resistors on the Interface PCA.

These Termination Resistors may or may not be used, depending on whether that particular drive is at the end of the Pertec-compatible Bus or not. The default configuration assumes that the drive (interface) is at the end of the Pertec-compatible Bus. The Termination Resistors are inserted in positions RP4 and RP5 and are "active." These resistor packs are identical and may be used in either position.

If the drive is being connected "in the middle" of the Pertec-compatible Bus, the Termination Resistors must be removed from the active RP4 and RP5 positions and should be stored in the "Spare RP4" and "Spare RP5" sockets.

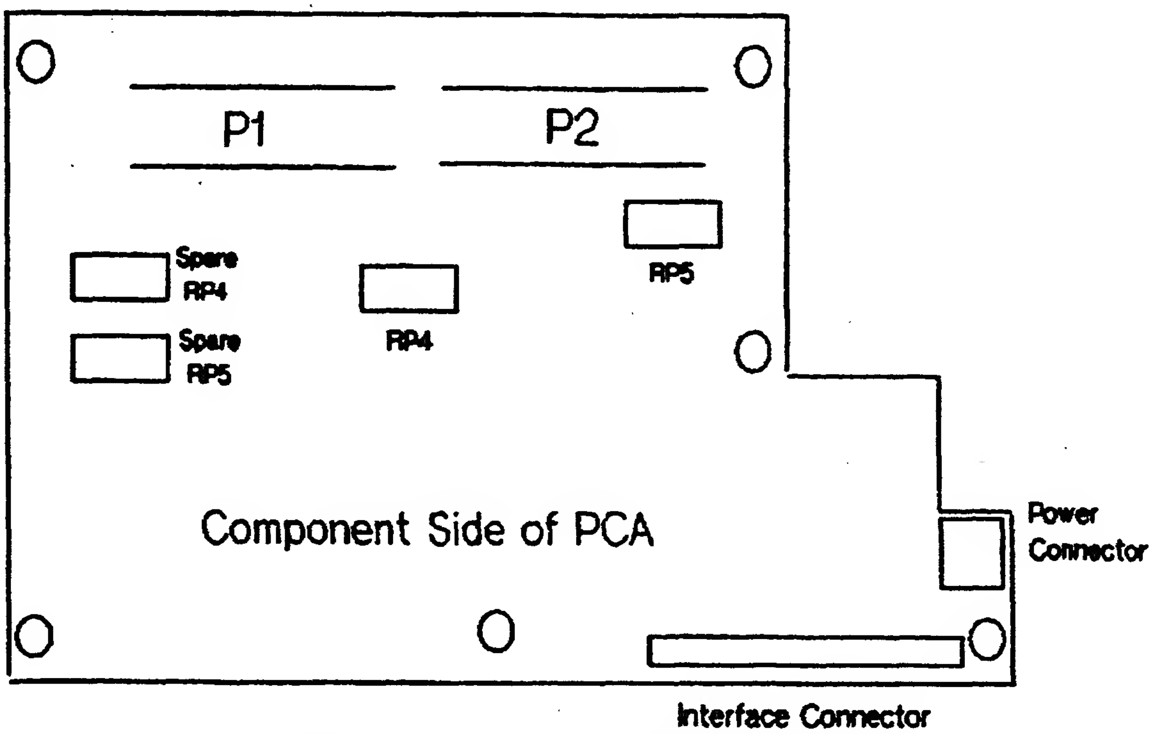

Figure 3-5. Pertec-compatible Interface

3.3 Reseating the PCAs

1. Make sure the power is off.
2. Remove the RFI cover on the top of the drive, exposing the PCAs.
3. Reseat all the PCAs.

3.4 Connecting Power and Switching On

Note

When transferring the tape drive from a very cold environment to a warm environment, or vice versa, it is very important to let the drive adapt to the new conditions to obtain maximum autoload performance.

Apply power to the drive for at least one hour before autoloading (Main AC Power Switch on the rear panel "1", Standby Switch on the front panel IN—see next NOTE). If the new environment is extremely humid or cold, allow at least two hours.

Tapes should also be acclimatized. Remove storage rings or cases and let the tapes set for at least one hour. If extremely humid or cold, allow at least two hours. This procedure allows temperatures to equalize and allows the tapes to dry out sufficiently to insure optimum autoloading.

For optimum read/write performance, allow the tapes to acclimate for 24 hours. This provides enough time for the tape humidity to equalize with that of the environment.

1. Connect the appropriate power cable to the power receptacle (110-120 V or 220-240 V cable).
2. Connect the power cable to the power source outlet.
3. Apply power by pressing the "1" on the **Main AC Power Switch.**
4. Press the **Standby Switch** on the front panel in (ON).

3.5 Clearing Non-Volatile RAM

1. Attach a jumper wire between the GND and CLRNV points on the Data Buffer PCA as shown in Figure 3-6.

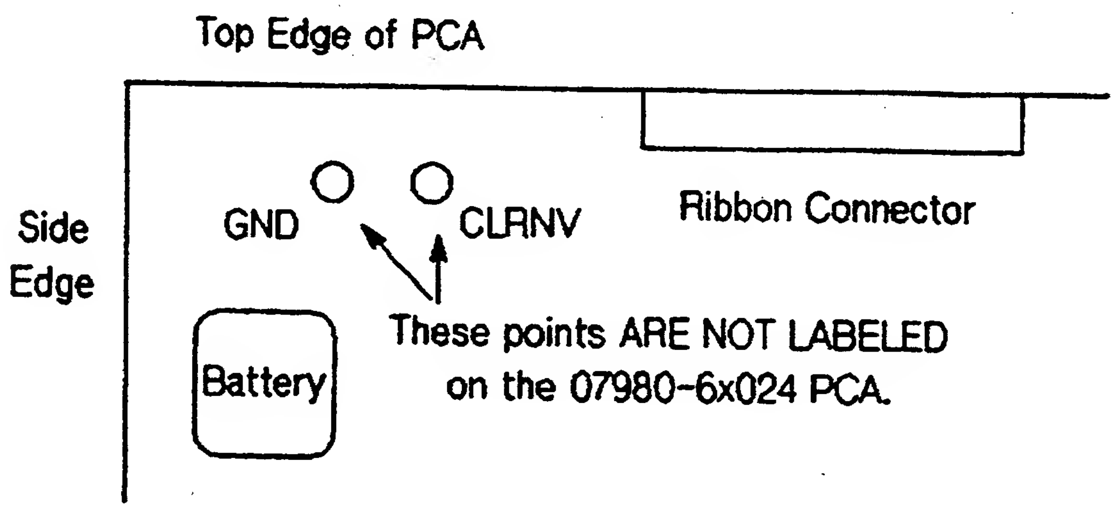

Figure 3-6. Data Buffer PCA GND/CLRNV Jumper Points

2. Apply power to the drive. After a few seconds, the display should show `FAIL 0`.
3. Remove power.
4. Remove the jumper from between GND and CLRNV points.
5. Apply power to the drive. Poweron test should PASS (drive will display `READY`).

Note

At this point, the NVRAM is clear and all configurations, including autogain values, must be reconfigured.

6. Replace the RFI cover over the PCAs.

3.6 Computing Autogain Values

Note

The read/write performance of the drive depends on how well the drive is tuned to cover the range of tapes used at a site. The factory setting of the gain values (as shipped) will most probably not be correct for the typical tapes found at any particular site.

1. Load a typical customer tape.

   Judgement should be used here to select a tape that represents the "mean" of the customer's tapes (rather than the "average"). Consider the range of tapes used (hot to cold), the relative amount of each "type" of tape used, and the age of each of these "types" of tape.

2. Run Test 99, press (ENTER) to choose `ONCE`, 1600, and `SAVE`.
3. (7980A/S; 7980XC/SX; 88780A/B) Run Test 99 again, choosing `ONCE`, 6250, and `SAVE`.
4. (7979A/S; 7980A/S; 7980XC/SX) If Option 800 is installed, run Test 99 again, choosing `ONCE`, 800, and `SAVE`.
5. (7979A/S;7980A/S;7980XC/SX) If Option 800 is installed, Load a "Master Skew" Tape, Run Test 105.
6. (7979A/S;7980A/S;7980XC/SX) If Option 800 is installed, Load a Scratch Tape, Run Test 106.

3.7 Setting the Address/ID Number

Your service representative will set the Address or ID number during installation. Use the following instructions should you ever need to change it.

1. Take the drive offline by pressing the [ONLINE] key.

   The Online Status Indicator should be dim.

2. Press [OPTION] to enter the Option Mode. `TEST *` appears in the display.
3. Press [NEXT] until `ADDR *` or `ID *` appears in the display.
   - `ADDR *` appears if you have an HPIB or Pertec-compatible interface.
   - `ID *` appears if you have a SCSI interface.
4. Press [ENTER].
5. Using [NEXT] or [PREV], bring the ADDRESS/ID number desired into the display.
6. Press [ENTER].

   The ADDRESS/ID you selected appears as `SET <#>`. The "#" is the address number (HPIB or Pertec-compatible) or the ID number (SCSI).

   This display lasts for one second and then returns to the `ADDR *` or `ID *` display (depending on the interface installed).

7. Leave the Option Mode by pressing [OPTION] or [RESET].

3.8 Storing Configurations

1. LOAD a short tape, with a write enable ring.
2. Run Test 150 to write an ID on the tape.
3. Run Test 128 to dump the non-volatile RAM to tape.
4. UNLOAD the tape. Mark the tape "STORED CONFIGURATIONS" or something similar.
5. Store the tape.

Note

Update this tape using the steps above when configurations are changed.

3.9 Operating the Tape Drive

Using the Control Panel

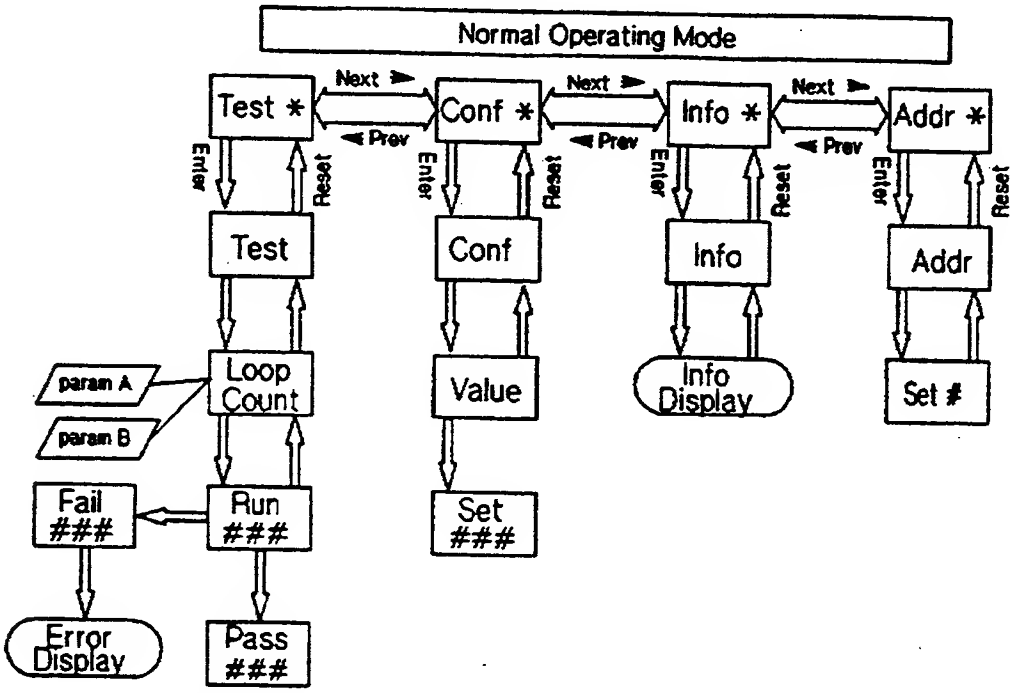

Figure 3-7. Front Panel Operation Flowchart

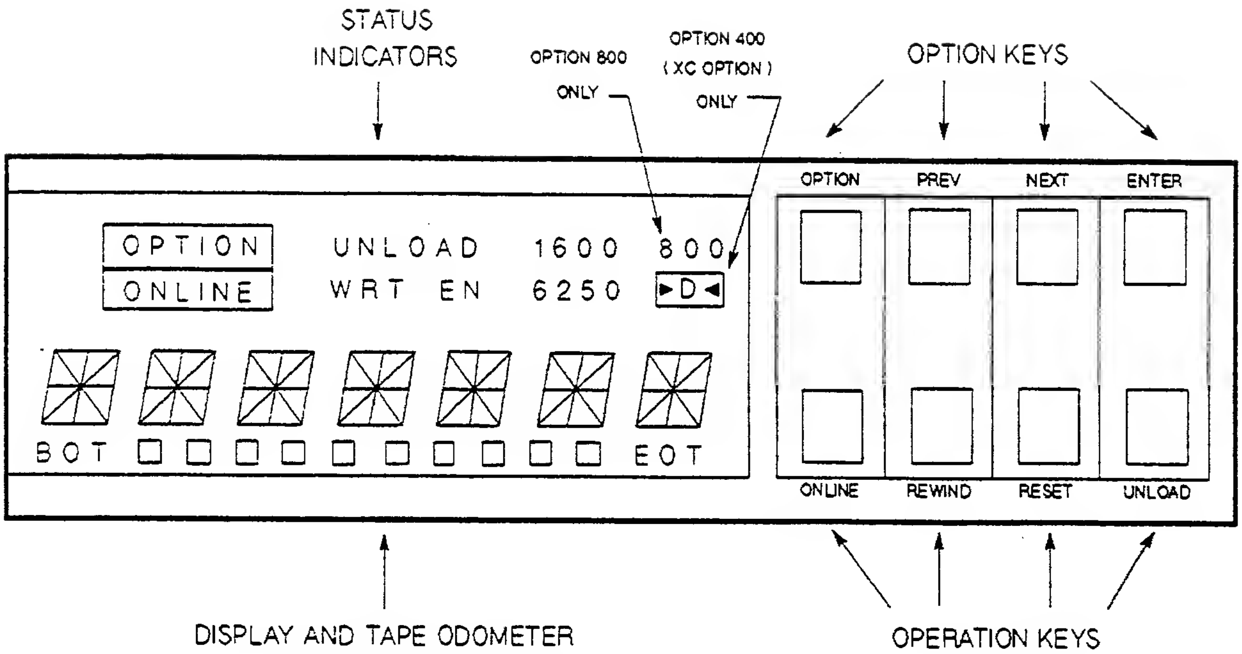

Figure 3-8. Control Panel for 7980

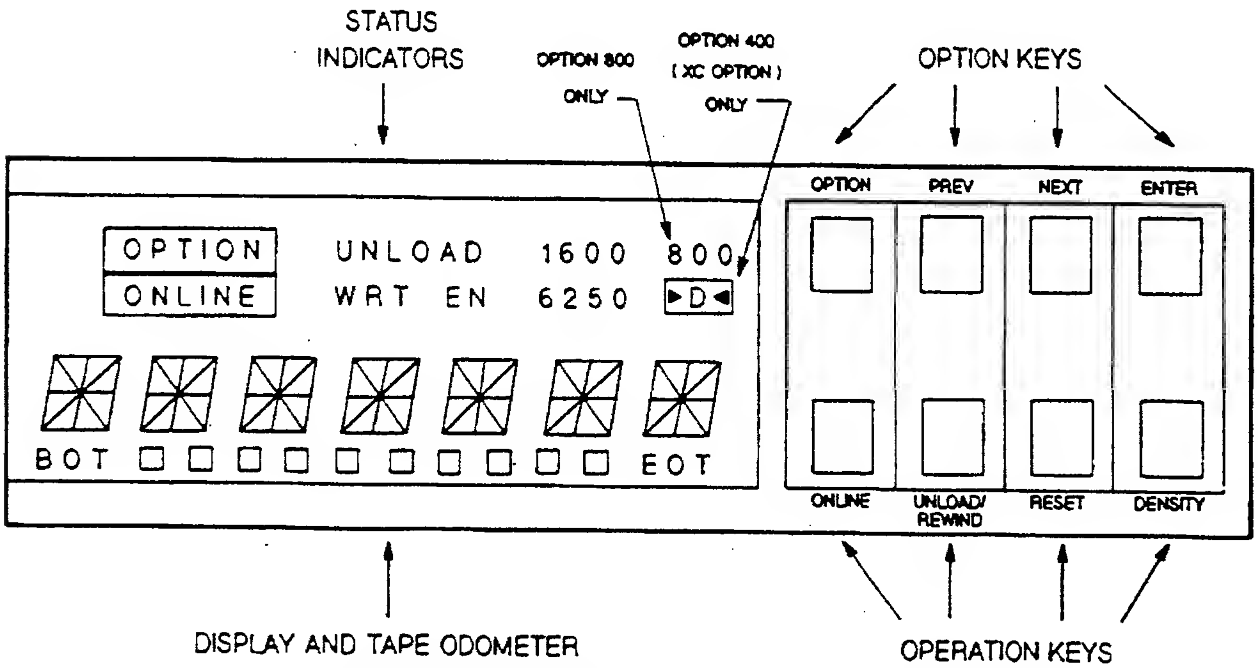

Figure 3-9. Control Panel for 88780

Table 3-1.
Control Panel Keys and Indicators
(Quick Reference to Basic Functions)

Control Panel Key	Function
Operation Keys	
ONLINE	Selects ONLINE or OFFLINE. Toggle key.
UNLOAD/ REWIND	(88780) One press - rewinds tape to BOT. Two presses - rewinds tape to BOT and UNLOADs tape.
UNLOAD	(7980) Unloads the tape and opens the tape door.
REWIND	(7980) Rewinds the tape to the BOT position.
RESET	Aborts an operation.
DENSITY	Selects write density.
Option Keys	
OPTION	Enters or exits the OPTION select mode.
PREV	Displays the previous OPTION choice.
NEXT	Displays the next OPTION choice.
ENTER	Selects the displayed OPTION and choices within the OPTION.

Table 3-1.
Control Panel Keys and Indicators
(Quick Reference to Basic Functions) (continued)

Control Panel Key	Function
Status Indicators	
OPTION	Lit when OPTION mode is selected.
ONLINE	Lit when the drive is ONLINE. Flashes if the ONLINE command is queued.
UNLOAD	Lit when an UNLOAD operation is in progress. Flashes if the UNLOAD command is queued.
WRT EN	Lit when a write-enabled tape is loaded into the drive. Remains on until tape is UNLOADed.
800	Lit when a 800 cpi write density is selected (Option 800 required).
1600	Lit when a 1600 cpi write density is selected.
6250	Lit when a 6250 cpi write density is selected.
>D<	Lit when a 6250 cpi write density with Extra Capacity is selected (Option 400 required).
TAPE ODOMETER	Segments show the relative position of the tape between the Beginning of Tape (BOT) and the End of Tape (EOT).

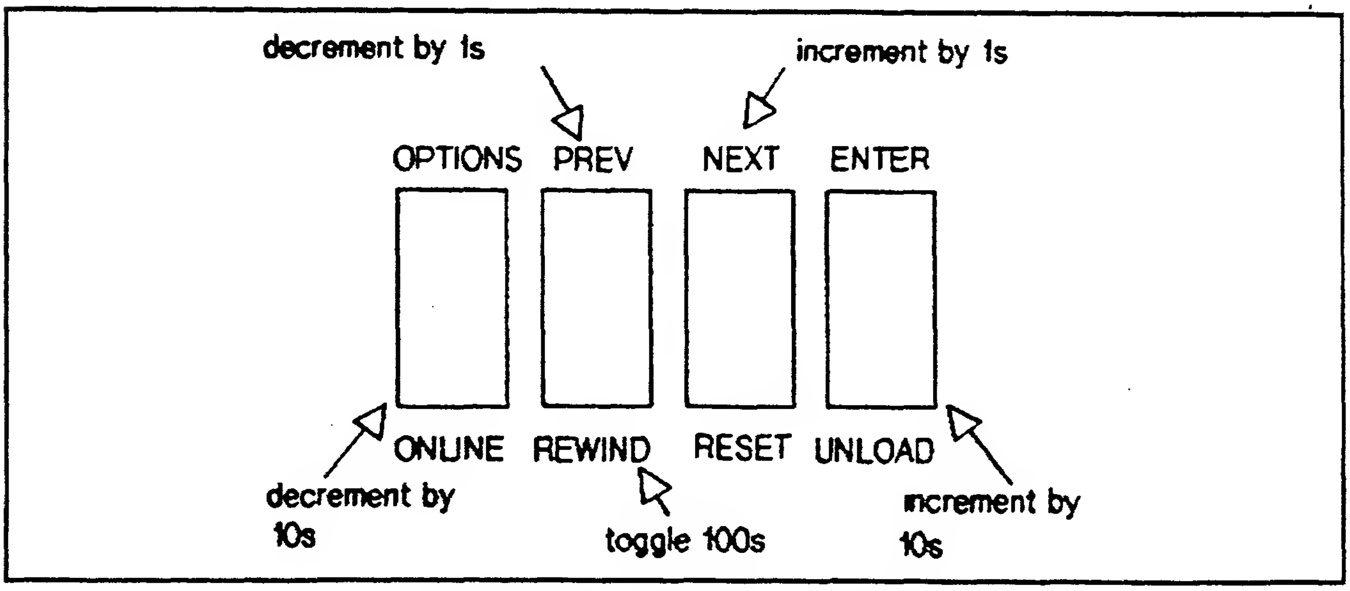

Figure 3-10. Key Tips for 7980

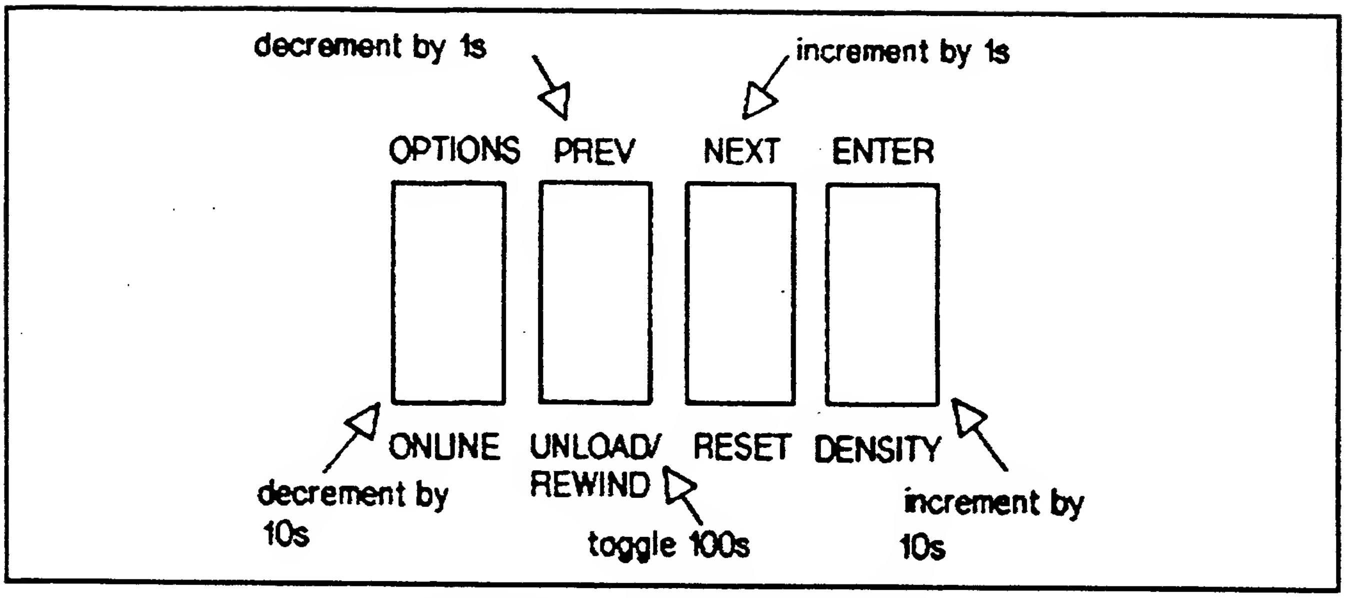

Figure 3-11. Key Tips for 88780

Operation Keys

Following is a detailed explanation of the control panel operation keys.

[ONLINE]

A toggle key that selects either ONLINE or OFFLINE operation of the drive. When the drive is ONLINE, it can accept and execute commands from the host. When the drive is OFFLINE, only local commands from the Control Panel can be executed.

The ONLINE status indicator lights when the drive goes ONLINE.

The ONLINE command may be queued; that is, you may press the key before the command can be performed, and the drive waits until the current operation is finished before going ONLINE. To indicate that the command is queued, the ONLINE status indicator flashes.

You may cancel a queued ONLINE command by pressing the [ONLINE] key a second time.

[UNLOAD/REWIND]

(88780) If a tape is between BOT and EOT and the drive is OFFLINE with the tape door closed, pressing the [UNLOAD/RELOAD] key *once* positions the tape at BOT.

When the BOT Marker is reached, BOT appears in the display.

Pressing the key *twice* (before the tape has rewound to BOT), initiates the REWIND sequence and queues the UNLOAD command. The tape continues past BOT, UNLOADs, and the tape door opens.

If the tape is at BOT when the [UNLOAD/REWIND] key is pressed, the tape UNLOADs and the tape door opens.

If no tape is in the drive, the door opens immediately when this key is pressed.

This key is inoperative if the drive is ONLINE or if the tape door is open.

UNLOAD

(7980) Pressing the UNLOAD key unloads the tape and opens the tape door. The UNLOAD status indicator lights. The key is active only when the drive is offline.

REWIND

Pressing REWIND positions the tape at BOT. When the BOT marker is reached, BOT appears in the display.

The REWIND key is inoperative while the drive is online or the tape door is open.

RESET

RESET aborts operations; both those from the Control Panel and those under control of the host (if BUSY is displayed).

Caution

Pressing the RESET key while BUSY is displayed causes the data in the drive buffer to be lost.

If the RESET key is pressed during a tape LOAD, the LOAD will be aborted—the tape door remains closed.

While in OPTION mode, pressing RESET backs up the selection process (and display) to the previous level.

DENSITY (88780) Used to change the write density.

This key is active before a tape is loaded or when a loaded tape is at BOT and the drive is OFFLINE. When pressed, DENSITY appears in the display (the density indicator corresponding to the current density selection is already on). (The density indicators which may be lit depend on the Options installed in the drive.)

The DENSITY key can be used to change the write density entered into the drive only while the DENSITY message is in the display.

While DENSITY is in the display, repeatedly pressing the DENSITY key causes the next density indicator, in turn, to flash.

If the ONLINE key is pressed within four seconds (to "enter" the density shown by the current flashing indicator) or if the DENSITY key is not pressed again within four seconds to select a different density choice, the drive accepts the density shown by the currently-lit density indicator.

Option Keys

Following is a detailed explanation of the control panel option keys.

OPTION OPTION activates the Option mode, lights the OPTION status indicator, and disables the Operation Keys.

You must first take the drive offline to enable the use of the OPTION key.

While in this mode, you may select options of TEST, CONFiguration, INFOrmation, or ADDRess (or ID).

Pressing the OPTION key while in any state except running a test or within the INFO display, returns the drive to normal, OFFLINE operation.

(PREV)	Pressing (PREV) decrements the number in the display or returns to the previous option.
(NEXT)	Pressing (NEXT) increments the number in the display or advances to the next option.
(ENTER)	Selects the OPTION currently shown in the display (TEST, CONFiguration, INFOrmation, ADDRess/ID).

Once an OPTION is selected, the (NEXT) and (PREV) keys are used to step through possible values for that OPTION and the (ENTER) key is used to select the value.

Status Indicators

Following is a detailed explanation of the Control Panel status indicators.

OPTION The **OPTION** indicator is lit when the drive is in OPTION mode and remains lit while you are accessing a particular option.

The **OPTION** indicator switches off if you press the (OPTION) key a second time.

ONLINE The **ONLINE** indicator remains on while the drive is ONLINE. This indicator flashes if the ONLINE command is in a queued state; caused by pressing the (ONLINE) key immediately after starting a LOAD sequence. When the LOAD sequence is finished, the drive will automatically go ONLINE and the **ONLINE** indicator will remain on continuously.

The **ONLINE** indicator switches off when you place the drive OFFLINE by pressing the (ONLINE) key a second time.

UNLOAD Lights when an UNLOAD operation is in progress. Goes out after the tape door opens in the UNLOAD sequence; `UNLOAD` appears in the display.

This indicator flashes if the UNLOAD command is queued. The UNLOAD command queues when either of the following situations occur:

- The (UNLOAD/REWIND) key is pressed while the tape is rewinding.
- The (UNLOAD/REWIND) key is initially pressed twice—first to rewind the tape if necessary, second to unload the tape.

WRT EN The **WRT EN** (Write-Enable) indicator lights, and remains on, when a tape with a write-enable ring is LOADed into the drive.

The **WRT EN** indicator switches off when the write-enabled tape is UNLOADed.

800 (Option 800 required) Continually lit to show that a 800 cpi write density has been selected.

During the density selection process, this indicator is flashed to show that 800 cpi density was selected.

1600 Continually lit to show that a 1600 cpi write density has been selected.

During the density selection process, this indicator is flashed to show that 1600 cpi density was selected.

6250 Continually lit to show that a 6250 cpi write density has been selected (or that a 6250 tape is loaded).

During the density selection process, this indicator is flashed to show that 6250 cpi density was selected.

This indicator is used along with the >D< indicator to show 6250XC selection. See description of the >D< indicator below.

>D< (Option 400 required) Continually lit to show that a 6250 cpi write density using Extra Capacity data storage procedures has been selected.

During the density selection process, this indicator, when flashed along with the 6250 indicator described above, shows that 6250XC (Extra Capacity) was selected.

TAPE ODOMETER Located under the seven-character display, the odometer consists of the BOT reference, a row of fluorescent segments, and an EOT reference. This display shows the relative position of the tape during operation.

Loading a Tape

Load the tape by completing the following steps:

1. Check that the tape you are loading has been acclimatized to room temperature and humidity.

   Remove storage rings or cases and let the tapes set for a least one hour after they have been in a different temperature and/or humidity level. If the temperature or humidity was extremely different, let the tapes set for at least 2 hours and, optimally, 24 hours.

2. Check that the end of the tape has been rounded and crimped.

   Autoloading should not be affected by small folds or irregularities in the last couple of feet of the tape leader. (The tape leader is the portion of tape between the physical end of the tape and the BOT marker.) However, if the leader has folds that run lengthwise along the tape or if that portion is definitely "crumpled", you should cut that part of the tape leader off.

   For best results use a tool made for cutting tape—like the tape cutter/crimper from Pericomp Corporation.

Note To ensure that the tape can be loaded on any drive that conforms to ANSI standards, do not shorten the tape leader to less than 14 feet.

---

3. Check that tape end is free to move.

4. Check for tape write-enable capability, as desired.

   Write-enable rings are installed on the back of a tape reel. When these rings are in place, you may record data on the tape. To PROTECT data from being over-written, REMOVE THE RING. You may then read data from the tape but are prevented from writing to the tape.

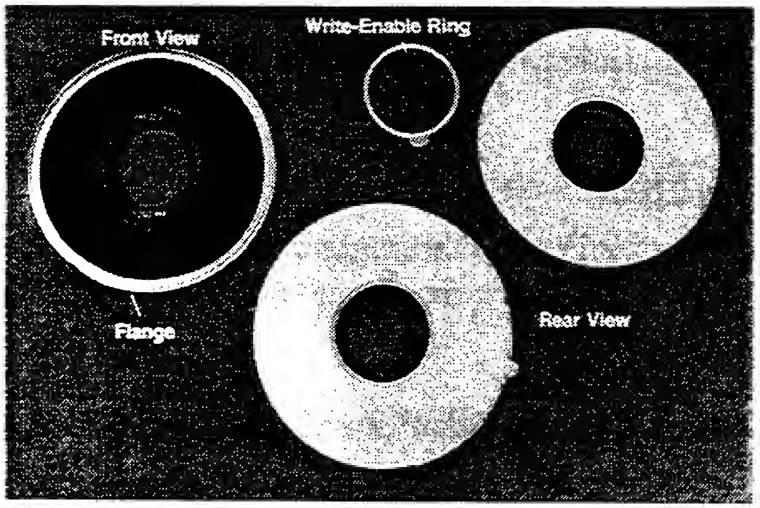

Figure 3-12. Write-Enabled and Write-Protected Tapes

5. Press the (UNLOAD/REWIND) or (UNLOAD) key to open the tape path door.

Caution Always press the (UNLOAD/REWIND) or (UNLOAD) key to open the door or to stop a LOAD operation. DO NOT TRY TO FORCE THE TAPE DOOR OPEN.

---

6. Slide a tape, free end to the right, into the center of the tape door opening.

   If inserting a small tape, it is best to insert the tape either to the center or a little to the right of center of the tape door.

   Make sure the tape leader is free on the right side of the reel, not trapped under the reel or by the tape path door.

7. Close the tape path door.

   You will see the following events:

   a. `LOADING` appears in the display.
   b. The write density of the tape displays (800, 1600, 6250, `BLANK`, or `UNKNOWN`). To detect and show the 800 cpi density, Option 800 must be installed.
   c. `BOT` displays.

8. Set the write density, if required, by doing the following steps. (Follow this procedure for 88780s. 7980 density selection is done from the host.)

   a. If the `ONLINE` indicator is lit, toggle the drive offline by pressing the (ONLINE) key.
   b. Press the (DENSITY) key.

      `DENSITY` appears in the display and the density indicator light for the current, selected density comes on (800, 1600, 6250, or 6250 along with the `>D<` indicator).

      Option 400 must be installed for the `>D<` indicator to light. Option 800 must be installed for the `800` indicator to light. This applies in the next step also.

   c. Press the (DENSITY) key again to light the desired density indicator.

      Each keypress lights the next indicator, in turn. The sequence is: 1600, 6250, 6250 with the `>D<` indicator (means 6250XC), and then 800.

      If the (DENSITY) key is not pressed within approximately five seconds, the drive automatically selects the density shown by the density indicator currently lit. The `DENSITY` message goes off.

   d. Press (ONLINE).

      The drive selects the density of the density indicator currently lit.

9. Press (ONLINE) (if not pressed during Density Selection).

   You may press the (ONLINE) key anytime after closing the door. You may queue the command to go ONLINE immediately after closing the door or wait until the drive finds the BOT marker. (Configuration 41 affects the affects the auto online feature.)

   You would press the (ONLINE) key immediately after closing the door if either 1) you knew that the current selection for write density was correct for your next write operation or 2) write density was not a concern for you at that time (i.e. you were only going to read a tape, not write).

   If you press (ONLINE) *before* loading has finished, the ONLINE indicator flashes and the drive waits to go ONLINE until loading is finished.

   If you press (ONLINE) *after* loading has finished, the drive goes ONLINE.

   When the drive goes ONLINE, the displays and indicators are as follows:

   - The ONLINE indicator remains lit.
   - The DENSITY indicator remains lit and shows the current selection for write density.
   - The WRT EN indicator remains lit and shows the write enable/disable status of the tape.
   - The message in the display generally corresponds to the command the host is currently sending to the tape drive.

Unloading a Tape

Follow these procedures to unload a tape (after it has been rewound).

1. Take the drive offline by pressing (ONLINE).
2. Press the (UNLOAD/REWIND) or (UNLOAD) key. The drive UNLOADs the tape and opens the tape door.
3. Remove the tape.

3.10 Control Panel Display Messages

Control panel display messages are divided into the following categories:

- Messages during normal operation (Table 3-2)
- Warning and error messages (Table 3-3)
- Idle operation and tape position messages (Table 3-4)
- Option selection messages (Table 3-5)
- Messages when within options (Table 3-6)
- Messages when within test option mode (Table 3-7)
- Messages during diagnostics (Table 3-8)
- Configuration value messages (Table 3-9)

Note

A question mark at the end of the message description means that the message is a prompt; what is shown in the display will be selected if the ENTER Key is pressed.

3.11 Messages During Normal Operation

Table 3-2. Messages During Normal Operation

Message	Description
□ □ □	The drive is powering up. All segments of all digits light.
TESTING	Displayed during poweron selftest sequence.
LOADING	The drive is LOADing a tape.
UNLOAD	The drive is UNLOADing a tape.
READING	The host is reading data from the tape.
RETRY	The drive is retrying an operation (88780).
WRITING	The host is writing data to the tape.
REWIND	The drive is REWINDing tape.
RESET	The drive is RESETting (commanded from either the Control Panel or the host).
DENSITY	The drive is waiting for a density selection from the Control Panel (88780).
6250	The tape LOADed into the drive has a density of 6250 cpi.
1600	The tape LOADed into the drive has a density of 1600 cpi.
800	The tape LOADed into the drive has a density of 800 cpi. (Requires Option 800.)
BLANK	The tape LOADed into the drive is blank.
UNKNOWN	A tape of unknown density was LOADed.
XC ON	(XC/SX Only) FLASHING-A density of 6250 cpi has been selected by the host and the drive is requesting a confirmation that the next write will be 6250XC. The operator may choose to select the alternative, industry-standard 6250 cpi, at this time by use of the NEXT or PREV key to display XC OFF and then pressing the ENTER key.
XC OFF	(XC/SX Only) FLASHING-A density of 6250 cpi has been selected by the host and the drive is requesting a confirmation that the next write will be industry-standard 6250 cpi. The operator may choose to select the alternative, 6250XC, at this time by use of the NEXT or PREV key to display XC ON and then pressing the ENTER key.

3.12 Warning and Error Messages

Table 3-3. Warning and Error Messages

Message	Description
BUSY	The drive is completing commands from the host. This display appears if the ONLINE or RESET Key is pressed while the drive is completing host commands.
WAIT	The drive is waiting for the interface to complete a request from the host. This message is displayed briefly.
ONLINE	A keypress on the Control Panel was received but cannot be accepted because the drive is ONLINE.
INVALID	The keypress received from the Control Panel cannot be executed in the present mode.
DISABLE	The host has disabled capability to remove the tape from the drive (88780).
MISLOAD	An attempt to LOAD a tape failed.
NO BOT	The drive could not find a Beginning-of-Tape (BOT) Marker.
INVERT	The tape was inserted upside down.
DOOR	The tape door or the top cover has been opened. This message is displayed if a Control Panel operation is attempted.

3.13 Idle Operation and Tape Position Messages

Table 3-4. Idle Operation and Tape Position Messages

Message	Description
`READY`	The drive is ready to accept commands or LOAD a tape. Whether this message or one of the next two messages (`NO TAPE` or `UNIT #`) appears in the display depends on the values stored in the Language Configuration (48). See NO TAPE and UNIT # described below.
`NO TAPE`	This message may be used instead of the `READY` message. See Language Configuration (48).
`UNIT #`	The "#" is the current bus address or ID. This message may be used instead of the `READY` message. See Language Configuration (48).
`BOT`	The tape is at the Beginning-of-Tape (BOT) Marker and is ready to accept commands.
`EOT`	The tape is beyond the End-of-Tape (EOT) Marker.
`[    ]`	The drive is waiting for a command. The tape is between BOT and EOT (but not at either one). If a command is not received in five seconds, the display changes to `IDLE` (see the next message description). This is not an error message.
`IDLE`	The drive is waiting for a command. The tape is between BOT and EOT (but not at either one) and a command has not been received in the last five seconds. This is not an error message.
`CHECK`	An excessive "soft" error rate has been detected by the drive. A "soft" error is anything that causes the drive to retry reading or writing a record. This message usually indicates that the tape path and head should be cleaned.

3.14 Option Selection Messages

Table 3-5. Option Selection Messages

Message	Description
TEST *	Selecting TEST Option?
CONF *	Selecting CONFIGURATION Option?
INFO *	Selecting INFORMATION Option?
ADDR *	Selecting Pertec-Compatible or HP-IB Interface ADDRESS number?
ID *	Selecting SCSI Interface Bus ID number?

3.15 Messages When Within Options

Table 3-6. Messages When Within Options

Message	Description
TEST###	Selecting test number
CONF###	Selecting configuration number
INFO###	Selecting information log number
SET ###	Configuration has been set to specified number
SET OFF	Configuration has been set to OFF (88780).
ADR OFF	PERTEC-compatible or HP-IB interface is set to OFF
ID OFF	SCSI interface is set to OFF

3.16 Messages When Within Test Option Mode

Table 3-7. Messages when within Test Option Mode

Message	Description
ONCE *	Run the selected test once?
10 *	Run the selected test 10 times?
100 *	Run the selected test 100 times?
1000 *	Run the selected test 1000 times?
LOOP *	Run the selected test until an error or until stopped by the operator?
RUN###	The drive is executing Test (###). (### = test number)
PASS###	Test (###) passed. (### = test number)
FAIL###	Test (###) failed. (### = test number)
A#####	Selecting parameter A(#####)? (##### = selected value)
B#####	Selecting parameter B(#####)? (##### = selected value)
SEQ39	User-defined sequence of tests is running.

3.17 Messages During Diagnostics

Table 3-8. Messages During Diagnostics

Message	Description
OPTION	OPTION Key name.
[ ]	ENTER Key name.
NEXT	NEXT Key name.
PREV	PREVIOUS Key name.
BOT EOT	BOT EOT sensor test message.
*	Sensor seen.
KEY *	Key test.

3.18 Configuration Value Messages

Table 3-9. Configuration Value Messages

Message	Description
**	Configuration value is unknown.
OFF	Select Configuration value of "OFF"?
ON	Select Configuration value of "ON"?
###	Select Configuration number value of <###>?
CLEAR	Select Configuration value of "CLEAR"?
SAVE	Select Configuration value of "SAVE"?
HOST	Select Configuration value of "HOST"?
REW *	Select normal, high-speed rewind?
ATC *	Select Archival Tape Conditioning rewind?

4

Preventive Maintenance

4.1 Cleaning Schedule Guidelines

Data integrity, tape drive performance, and longevity of your tape library can be maximized if you do the following:

- Keep the tape path and tapes clean.

  Taking preventative measures is in your best interest. A clean tape path and clean tapes reduce read/write errors, shorten read/write times, lengthen tape life, and translate into less work for you.

- Care for the tapes properly.

  Handling, storing and transporting tapes correctly prevents edge damage, reel failure, and tension loss.

- Select and use high-quality tapes.

  HP strongly recommends the use of its premium quality tapes to maximize data integrity and reduce the frequency of replacement.

- Keep the environment of the tape drive and tape storage area clean.

  A clean room environment with carefully controlled temperature and humidity is the optimal environment for your tape drive and tapes.

4.2 Cleaning the Tape Path and Tapes

In this section you will learn the following:

- How often to clean the tape path.
- What cleaning supplies to use.
- How to clean the tape path and the tapes.

Cleaning Schedule

How often you clean the tape path depends on usage, operating environment, and tape quality.

Typically you will need to clean the tape path once every eight hours. However, if the error message `CHECK` occurs regularly, you should clean the tape path more frequently. If frequent cleaning does not improve reliability, check your tapes. Are the tapes old, worn, or kept in a dirty area? All old and worn tapes should be copied immediately and then discarded. You should evaluate tapes regularly.

The definitions in the following chart should help you develop an appropriate cleaning schedule.

Table 4-1. Cleaning Schedule Guidelines

Cleaning Level	Cleaning Criteria
MINIMUM	Clean the tape path thoroughly EVERY EIGHT HOURS if: ■ Less than ten reels are used in eight hours. ■ You see no particles on the tape head after each reel of tape. ■ You do not suspect abnormal dust in the computer room from increased traffic or vacuuming.
NORMAL	Clean the tape path thoroughly EVERY ONE TO TWO HOURS of continuous running if: ■ More than ten reels are used in eight hours. ■ You see no particles on the tape head after each reel of tape. ■ You do not suspect abnormal dust in the computer center.
HEAVY	Clean the tape thoroughly AFTER EACH REEL of tape if: ■ Particles appear on the tape head after each reel of tape. ■ You are reading interchange tapes from outside your computer center. ■ You are using new or little-used tapes. (New tapes usually contain debris from the slitting process during their manufacture.)
SPECIAL	Clean the tape path ANYTIME that you suspect abnormal dust in the computer center because of custodial activity, equipment moves, supply delivery, of if the drive has not been used for several days.

Cleaning Supplies

Cleaning supplies are available from Hewlett-Packard. See Chapter 1 "1.5 Accessories" for ordering information.

Use these materials to clean the tape path:

- Cleaning solvent

  Hewlett-Packard supports only high-quality electronic-grade isopropyl alcohol of at least 90% concentration. The isopropyl mixture must consist of alcohol and distilled water only.

- Non-Abrasive, lint-free cloths and/or swabs

Caution

- ☐ Do not use cleaner solutions that contain lubricants. Lubricants deposit on the tape head and impair performance.
- ☐ Do not use alcohol cleaning solutions on the rubber gripping fingers on the takeup reel.
- ☐ Do not use aerosol cleaners. The spray is difficult to control and often contains metallic particles that can damage the tape head.
- ☐ Do not use soap and water on the tape path. Soap leaves a thick film, and water may damage electronic parts.
- ☐ Discard the cloths and swabs after use. Even if they appear clean, they are contaminated.
- ☐ Do not use facial tissues. Although they may seem effective, they leave highly abrasive lint in the tape path.

Cleaning Procedures

Figure 4-1 illustrates the points within the tape drive you should clean periodically.

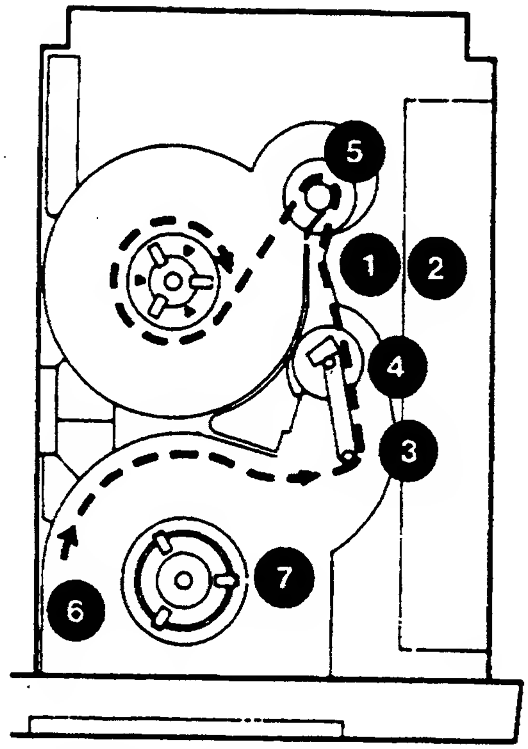

Figure 4-1. Cleaning Points

1	Read/Write Head
2	Cleaner Block
3 through 7	Tape Path

Before You Begin

Gather your cleaning supplies and note the following cautions.

Caution

- If you have to transfer the cleaning solvent to another container, use only a clean, unwaxed container.

  Alcohol dissolves wax. If you use a waxed cup, the wax transfers to the tape path.

- DO NOT dip your cloths and swabs into the cleaning solvent container or touch the cloths or swabs to the lip of the open container during pouring. Doing so contaminates the solvent.

Cleaning the Read/Write Head

With a new swab or wipe moistened with cleaning solvent, do the following steps.

Note

If you are using a swab or a Texsleeve®, keep the stick vertical so that you contact all of the head.

---

1. Wipe the head using at least 15 firm strokes up and down (perpendicular to the casting).

   Be sure to clean all of the head; do not overlook the portion of the head nearest the casting.

2. Using a clean portion of the wiping material, use at least 15 firm strokes left/right (in the direction of tape motions).

   Always finish with a left/right cleaning motion.

3. Change the swab or sleeve and repeat cleaning until you cannot see any trace of debris on the cleaning material.

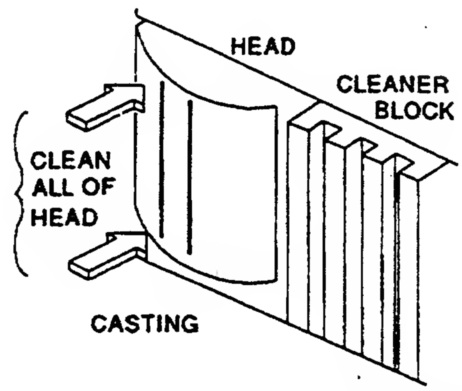

Figure 4-2. Cleaning the Read/Write Head

Cleaning the Cleaner Block

Note

Swabs or the edge of a Texsleeve; fit in the grooves of the cleaner block very well.

1. With new cleaning material, moistened with cleaning solvent, clean the cleaner block using firm strokes.
2. Change your cleaning material and repeat cleaning until you cannot see any trace of debris on the swab.
3. Finish by wiping the cleaned surfaces of the cleaning block with a clean swab or wipe moistened with cleaning solvent.

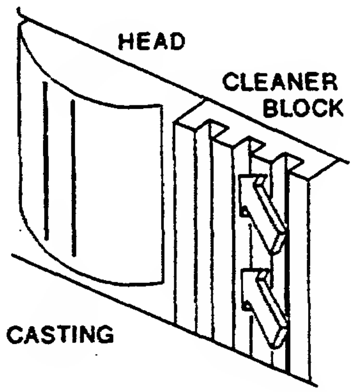

Figure 4-3. Cleaning the Cleaner Block

Cleaning the Tape Path

Each of the remaining tape path points need to be wiped clean.

1. Using a new swab or wipe moistened with WATER, clean point #7, the rubber gripping fingers.

   Do not use cleaning solvent on rubber.

2. Using a new swab or wipe moistened with cleaning solvent, clean the remaining points #3 through #6.
3. Allow the tape path to dry for at least 30 seconds before loading a tape.

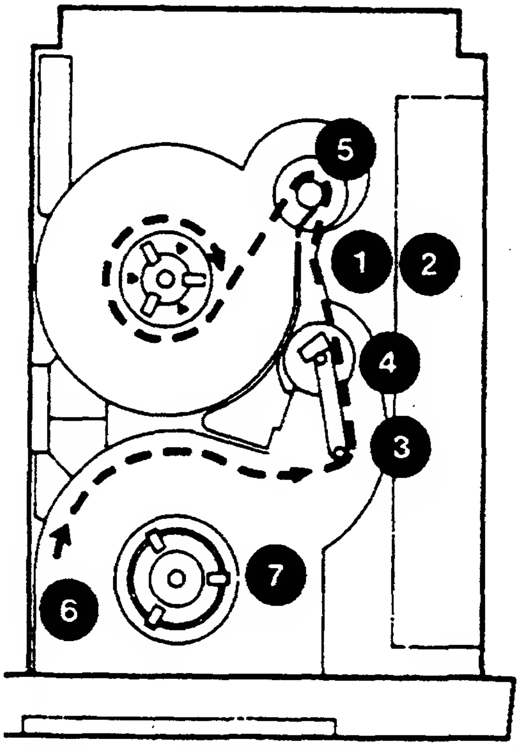

Figure 4-4. Cleaning the Tape Path

Cleaning Tapes

Ideally, you should clean your tapes with a cleaner/certifier machine. The cleaning process begins when adhered debris (wound into a reel of tape under extreme surface pressures) is loosened. Once debris is loosened, the debris is scraped from both sides of the tape.

Caution

If you choose to use a tape cleaner/certifier machine that uses tissues, do not use lubricated tissues. They may leave a film and may damage the tape and tape drive.

Also be sure the tissues are of high quality and are lint-free. Do not re-use portions of the tissue rolls. This leaves the tape dirtier than when you started.

Note

Tape cleaners should **not** be considered a substitute for the following:

- Using high-quality tapes
- Maintaining a clean tape path and heads
- Maintaining a clean environment for the tape drive

New Tapes

New tapes can contain debris from the manufacturing process, so Hewlett-Packard recommends that new tapes be conditioned before use. Either clean the new tape using the cleaner/certifier machine; or, load the tape into the tape drive and run it end-to-end.

If you use the tape drive cleaning method, you must be sure to clean your tape drive thoroughly after this process.

4.3 Managing and Caring for Tapes

Using high quality tapes and following these guidelines prevents errors and lengthens the life of your tapes. Poor tape practices cause many failures.

The following topics are covered in this section:

- Storing tapes
- Transporting tapes
- Handling tapes
- Rewinding tapes
- Evaluating tapes
- Labeling tapes

Storing Tapes

- You may choose to use the Archival Tape Conditioning feature to improve tape stacking for storage.
- Keep tapes in a clean environment at all times. Exposure to dust and other particles such as food and cigarette smoke impairs tape performance. Choose storage areas away from office activity to reduce contamination.
- Maintain a constant temperature around 70°F (21°C) and a relative humidity around 40%. Tapes subjected to extremes in temperature or humidity may become sticky or brittle.
- Do not stack tapes horizontally unless they are in metal canisters.
- Secure the end of the tape by a vinyl strip or a foam pad to prevent tension loss. DO NOT use adhesive tape because it can leave a sticky residue.
- During long-term storage, reduce contamination by sealing canisters in plastic bags. BE SURE TO REMOVE DUST ON THE OUTSIDE OF THE BAGS BEFORE REMOVING THE CANISTERS.
- Always remove the tape from a tape drive destined for storage or extreme temperature/humidity. The tape can stick to the head if it is left in a non-operating environment tape drive.

Transporting Tapes

- Avoid physical shock and extreme temperature changes.
- Pack tapes in water-resistant containers when you are moving tapes from one location to another.
- Secure the ends of the tape to maintain proper tension.
- Avoid metal detection equipment (such as the kind in airports), because electromagnetic fields can be strong enough to cause data loss.

Handling Tapes

- Hold the tape reel by the hub or as close to the hub as possible.

  Use care when handling the tape reels. If reels are gripped in any way that presses the flanges together, there is a possibility of damaging the edge of the tape.

  The hub is the strongest, least flexible portion of the reel. ALWAYS HOLD THE TAPE REEL BY THE HUB OR AS CLOSE TO THE HUB AS POSSIBLE.

  There is a greater danger of mishandling tape reels when using a horizontal-mount tape drive. The figure below shows how to hold a reel in a horizontal position with one hand without pressing the flanges together.

NO YES

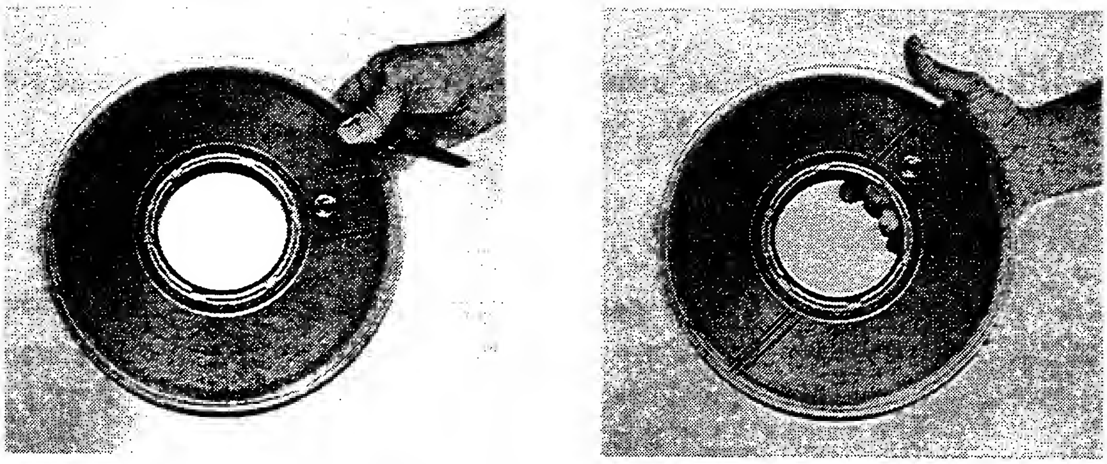

Figure 4-5. Preventing Tape Edge Damage

- Do not pick up the reel by the flanges; they are easily bent. If the flanges are bent, the tape may unwind unevenly, which can eventually cause edge damage.
- Do not shake the tape. Shaking causes pack slip.
- Prevent sharp blows to the reels. The reel could fracture and damage the tape.

Rewinding Tapes

Proper tension is necessary to ensure smooth movement of the tape and accurate data transfer. Excessive tension permanently distorts the backing, while loose tension causes cinching. A properly maintained tape drive will rewind tapes at the correct tension.

- To prevent the pack from losing its tension, secure the end of the tape with either a vinyl strip or a foam pad when you remove it from the drive.
- Tapes can be contaminated if they are wound onto dirty reels. Clean empty reels before using them.
- Adopt a program of regular inspection, winding, and rewinding of stored tapes every six to nine months to ensure wind quality.

Evaluating Tapes

You can stop your system from wasting valuable time retrying and skipping bad sections of tape by evaluating your tapes regularly. Reels of tape should be discarded once they reach one or more of the following levels:

- 150 single-track errors every 2400 feet
- 10 total (in any combination) two- and three-track errors every 2400 feet
- 1 permanent write error every 2400 feet.

These are maximum error rates. Please evaluate your tapes using whatever system or program is available to you, but set your levels low to prevent data loss and retries.

Labeling Tapes

To run a well-managed tape library, you must keep accurate records of each tape's condition and adopt a regular schedule of evaluation. This will help you ensure reliability, lengthen tape life, and spot problems quickly.

Use reliability labels, similar to the one in the following figure, to reduce paperwork and increase your efficiency. The labels eliminate files, since they allow you to record a tape's history on the reel itself. You need only glance at the label to identify the condition of the tape and determine when maintenance is required.

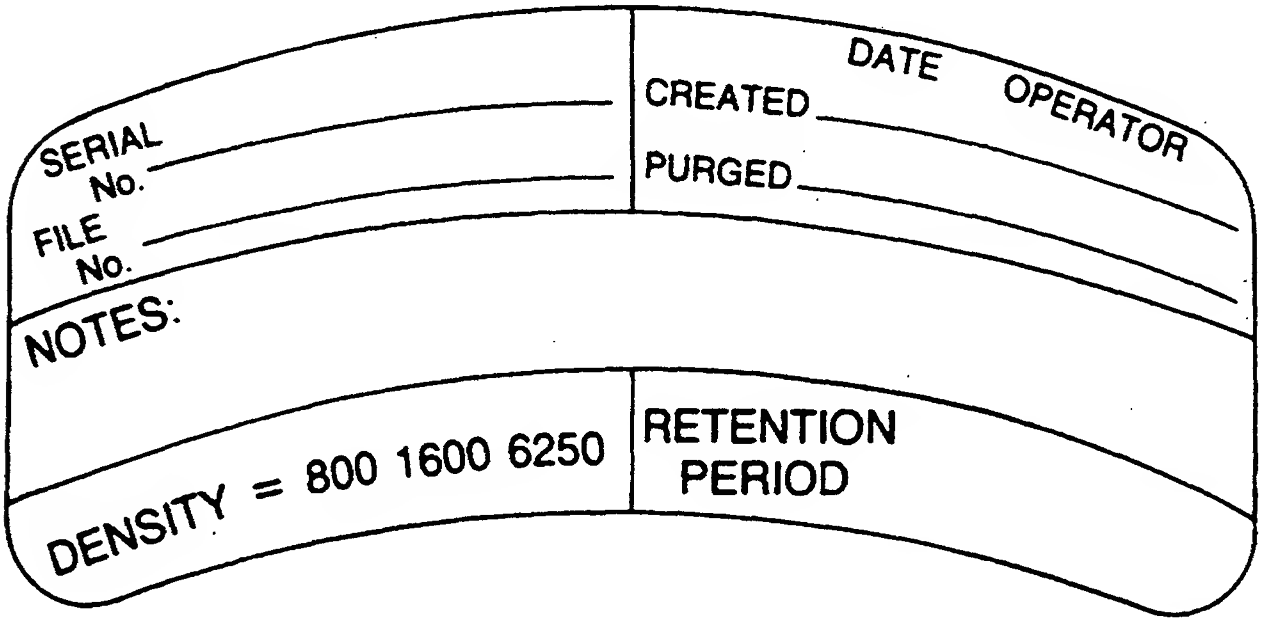

Figure 4-6. Example of a Tape Reliability Label

Special care must be taken with tapes written in 6250XC format (Option 400). This format is intended for large backups and is not generally used for interchange unless the interchange party has an HP 88780B with Extra Capacity storage capability (Option 400 installed). One other tape drive that may be used by the interchange party is an HP 7980XC/SX. It is recommended that you mark tape labels with "6250XC" if the Extra Capacity feature is used.

This labeling can be done manually on the tape label or placed in the "Comments" field of an automated tape library manager.

Labeling tapes is especially important in an installation that uses several different types of tape drives. Although the HP 7980XC/SX and 88780B with Option 400 recognize and are able to correctly expand the data automatically, other tape drives only recognize that the tape is a 6250 cpi tape; a host error will be returned when reading is begun.

Operators should be trained to mount 6250XC tapes only on Extra-Capacity-capable tape drives when data is to be read back. (Of course, ANY tape may be mounted on ANY tape drive for a write.)

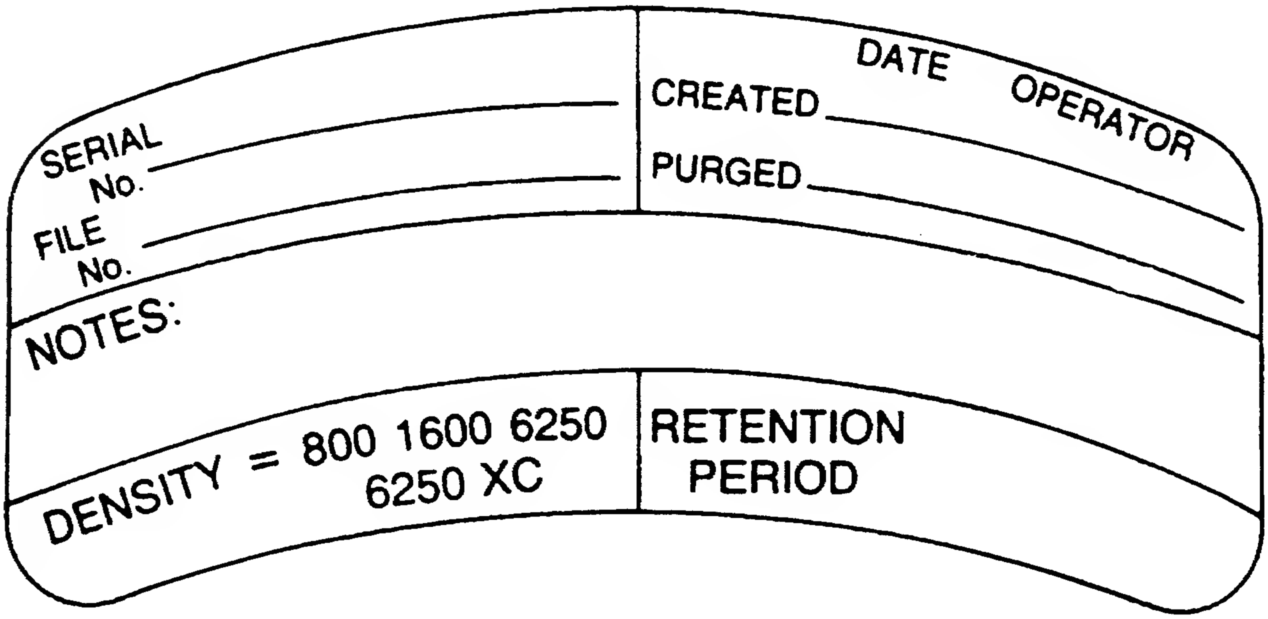

Figure 4-7. Suggested Extra Capacity Reel Label

Resources

If tape and tape path problems persist after following all the suggested procedures and practices in this chapter, call your nearest Hewlett-Packard distributor. The tape drive may need to be repaired by a service engineer.

The following publications are available for those who wish to learn more about tape care and library management:

- *Care and Handling of Computer Magnetic Storage Media*, Sidney Geller, National Bureau of Standards Special Publication #500-101, 1983.

  Contact:

  Superintendent of Documents
  U.S. Government Printing Office
  Washington, D.C. 20402

- *The Handling and Storage of Computer Tape*, 3M Company.

  Contact:

  Technical Service
  Data Recording Products Division
  3M Company
  3M Center
  St. Paul, Minnesota 55101

- *Success With Magnetic Tape*, Hewlett-Packard Company, HP P/N 5953-7131.

  Contact:

  Hewlett-Packard Direct Marketing Division
  1320 Kifer Road
  Sunnyvale, CA 94084
  (800) 538-8787 in U.S.
  (406) 738-4133 in Alaska, California, or Hawaii

4.4 Selecting Tapes

Note

The selection and use of media, supplies, and consumables are the customer's responsibility. Hewlett-Packard reserves the right to exclude from the warranty or service agreement any repairs for damage to HP products which HP reasonably determines or believes was caused by use of non-HP media or cleaning supplies. Hewlett-Packard will, upon request, repair such damage on a time and material basis.

You may purchase tapes directly from Hewlett-Packard. Refer to Chapter 1 "1.5 Accessories".

5

Functional Description

The following sections are in this chapter.

5.1 Overview

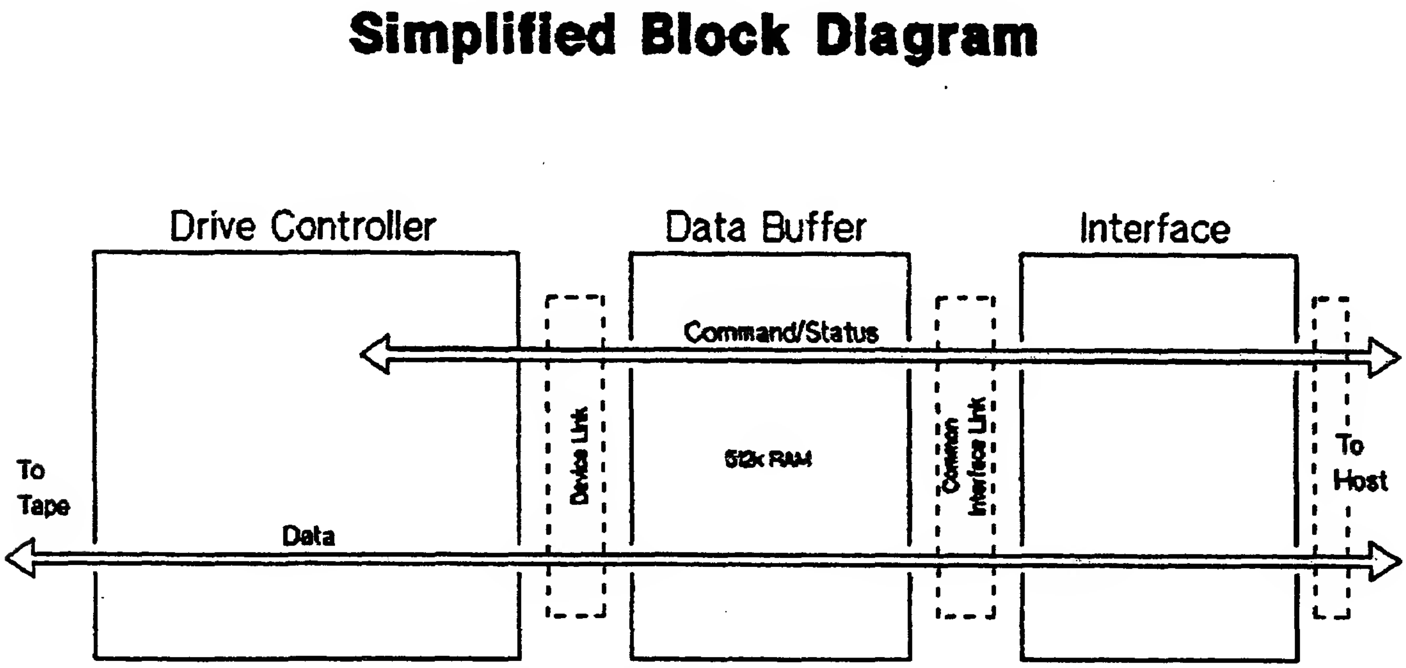

Figure 5-1. Simplified Block Diagram

General Theory of Operation

The following is a generalized sequence of events that occur when the drive Reads or Writes data. Included is an explanation of some of the 7978A/B performance enhancements that are used in the drive. These features include Immediate Reporting, Readaheads, and Error Recovery (retries) by the data buffer.

The Host computer communicates with the tape drive over the interface hardware link using an interface dependent protocol. A Write (or Read) Record command is first sent to the tape drive. The drive's tape transport mechanism accelerates the tape from its stationary state towards its Read/Write speed (125 ips for the drive). As the transport approaches the targeted speed, the interface hardware/software notifies the Host that the Write data must be sent across the interface. The interface then opens the path into the Data Buffer so the Buffer can transfer data from the Host into the Buffer memory.

Meanwhile, when the transport reaches the target speed, and when the erase bar on the head is positioned in the gap past the end of the last record written, the erase current is turned on. After at least the minimum size gap has been erased, the electronics in the transport mechanism transfers data from the Data Buffer (originally from the Host) into its Formatter which encodes it into the proper format (PE or GCR). The data is then converted into flux reversals that are written onto the tape.

Once all of the data for this record has been brought in from the Host and written onto tape, the transport mechanism's electronics erases a gap following the record just written. If another Write command has not been issued by the Host, the mechanism stops the tape.

While the drive is Writing data to tape, the Read gaps on the head detect the data, after it has been written on the tape, and verifies that the data was written accurately. This is done by reading the data and performing an error detection routine without actually transferring the verified data into the Data Buffer.

If the Read electronics detects an error while Writing, the record must be re-written. The 7979A/7980A, and the 7978A/B automatically do this for the Host. Earlier generation drives, such as the 7970, simply report an error to the Host and make the Host issue a series of commands to the drive to make it reposition, and subsequently re-write the data. (The Host had to re-transmit the Write data).

Many of the older tape drives that do not have a Data Buffer at least had a FIFO which allowed them to match the speed between the Host transfer rate and the transport mechanism transfer rate, described above. Other older drives, however, do not even have a FIFO. Hosts using these drives MUST provide data at exactly the correct time. Incorrect timing produces an underrun error; in such a case, the data must be re-written.

The sequence of events for a Host-initiated Read is almost identical to a Write. The major differences are:

1. The Write and Erase electronics are not activated
2. The direction of data transfer is reversed. The drive can Read the entire record into the buffer (assuming the buffer is big enough), and will transmit the data to Host if the data is good. (The 7978A and 'B' do this also.)

The data read is transmitted to the Host before the read of the record has completed as long as: the data buffer is larger than the record, and there is data in the drive (no FIFO) so that speed matching between the Host and drive can be made. If the Read fails, the Host must tell the drive to re-read the data.

The interface electronics receives the Write command from the Host computer. The Write command is separated into two lower level commands (Write Request and Execute Write), which is passed to the Data Buffer. The Write Request command is then passed to the Drive Controller, which brings the tape up to operating speed. The Drive Controller then returns a Completion Status to the Interface via the Data Buffer.

The Interface needs to wait for the Completion Status before issuing the Execute Write command. Data must not be brought in from the Host until this command is issued, because the Data Buffer will not transfer in data until it receives Execute Write. Once the data for the record is all in the buffer, the Data Buffer sends the Execute Write command to the Drive Controller. The Controller takes the data from the buffer, formats it, and physically writes it onto the tape.

When the writing operation is complete, the Drive Controller writes (erases) a gap following the data, and then repositions for the next operation Completion Status is then returned to the Interface via the Data Buffer, followed by a completion signal from the interface to the Host.

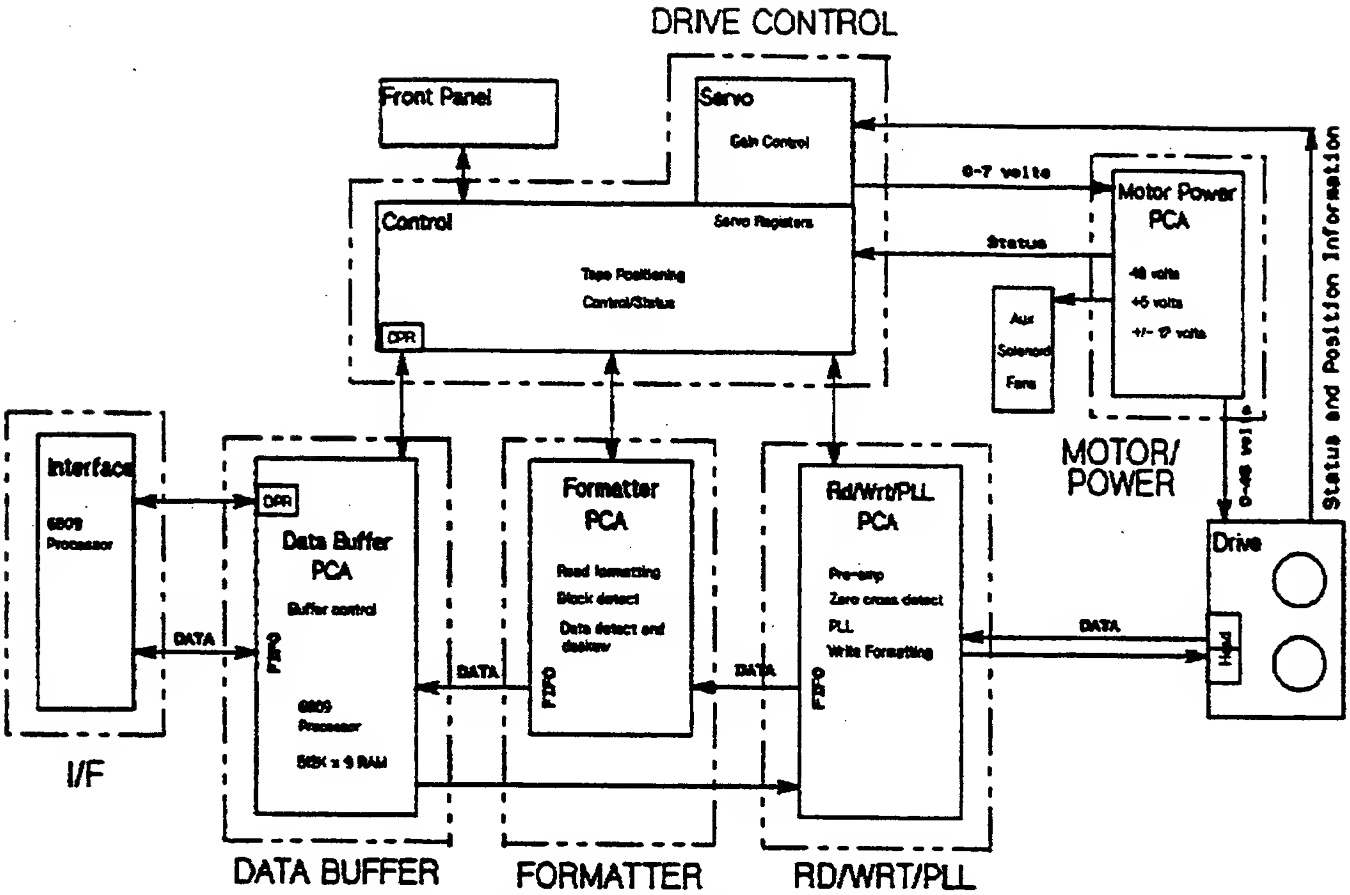

Figure 5-2. Overall Block Diagram (four PCA version)

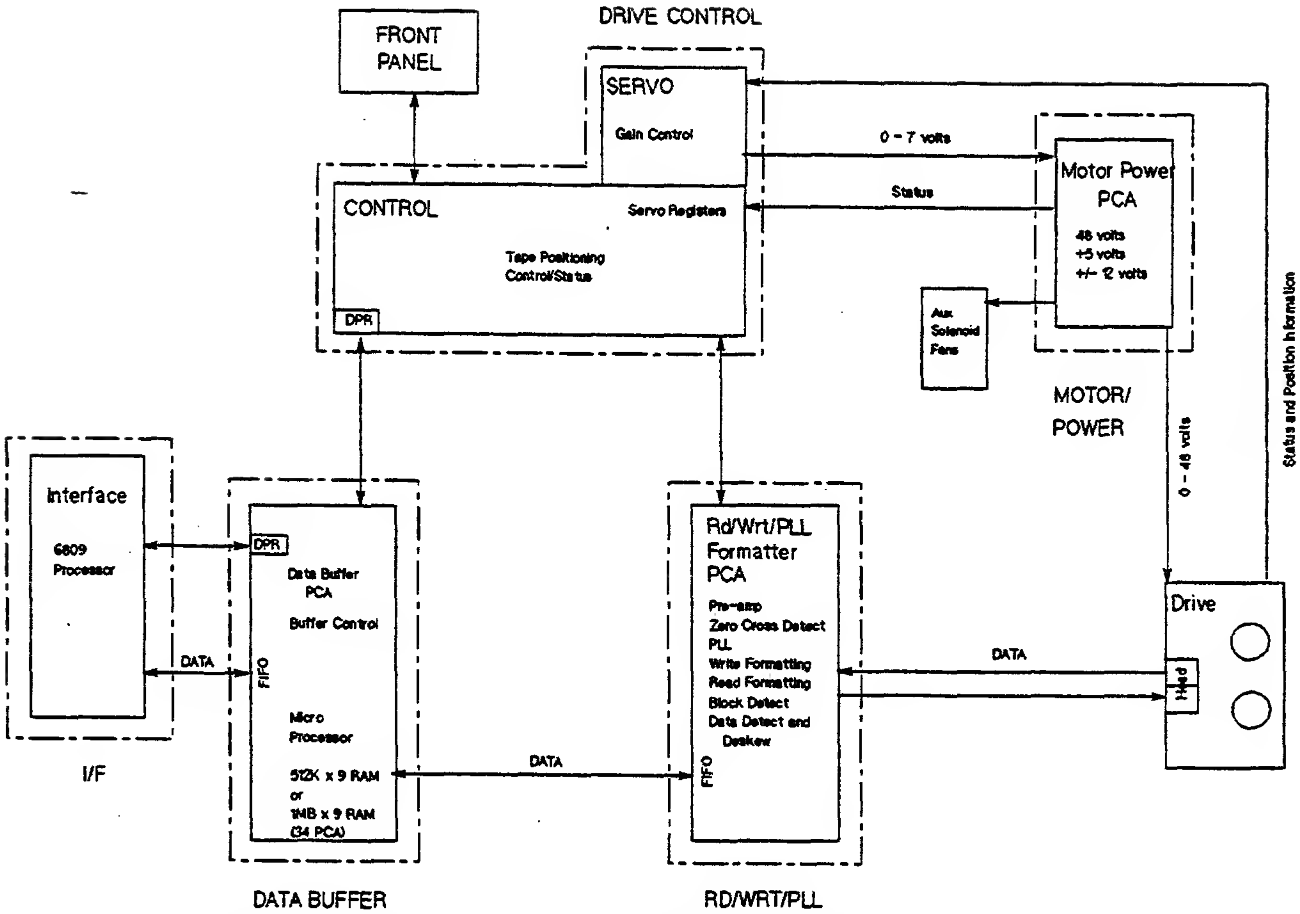

Figure 5-3. Overall Block Diagram (three PCA version)

Read commands are NOT broken into two separate commands by the Interface. When the Host issues a Read, it is ready for the data. The Interface passes the Read to the Drive Controller via the Data Buffer. When the Drive Controller has finished bringing the Read data into the Data Buffer, the Buffer starts transferring the data to the Host. Completion Status is given when the operation is complete.

When the Drive Controller sees that a Read or Write error has occurred, it issues Write and Execute Write (or Read) commands until the operation completes without error, or until the retry count (nominally seven) expires. Either "Corrected Error" or "Hard Error" will be returned to the Host via the interface when the Retry operation is finished. No Completion Status will be sent to the interface by the Data Buffer until the operation is successful (first time data transfer or after expired retries).

In addition to the retry mechanism built into the Data Buffer, the drive uses two additional performance features: Immediate Reporting when writing, and Readaheads. These features allow the Data Buffer to queue up Write and Read commands for the Drive Controller when Reading. The Drive Controller will always have a Write Command ready for it after writing the gap following the data, and thus won't have to reposition; it "streams."

How does this Immediate Reporting work? Once the drive is in Immediate Reporting mode (Host Command, Front Panel selectable, and/or Default Mode), the Data Buffer immediately issues Completion Status back to the Interface over the Common Communication Link (CCL) when it receives the Write Command. This tells the interface to enable the Host to transfer Write data into the drive and issues an Execute Write command to the Data Buffer.

The Data Buffer transfers write data into the buffer memory at the Host transfer rate. A Completion Status is issued to the Interface IMMEDIATELY after the last byte is in the buffer memory. The Host repeats the process by sending another Write command to the drive.

The Data Buffer determines when to issue the first Write command to the Drive Controller by looking at the buffer memory size, the incoming data size and data rate of the records coming from the Host. When the Drive Controller is up to speed, it returns Completion Status to the Data Buffer via the Device Link. The Data Buffer immediately issues an Execute Write command to the Drive Controller, which transfers data from the buffer memory at the rate of 781,250 bytes/s (6250*125 ips) for GCR.

When the Drive Controller completes writing the data and gap, it issues Completion Status to the Data Buffer; the Data Buffer then IMMEDIATELY sends another Write command to the Drive Controller. Since the Drive Controller is already at speed, it immediately sends Completion Status to the Data Buffer, which then sends an Execute Write command to the Drive Controller. The Data Buffer is always queueing Write data from the Host, and transferring it to the Drive Controller. It keeps the drive "streaming" by speed matching the Host and Drive Controller transfer rate with buffer memory rate.

Readaheads work in the same way, except that the data transfer is in the opposite direction. It starts with the Host instructing the drive to Read. The Interface issues this Read to the Data Buffer, which then passes it to the Drive Controller. Once the Tape is at operating speed, it transfers the data into the buffer memory, and issues Completion Status to the Data Buffer. The Data

Buffer allows the host to transfer the data via the Interface and passes the Completion Status to the Interface when the transfer is completed.

Meanwhile, the Data Buffer has immediately issued another Read command to the Drive Controller when it received the Completion Status, and the Drive Controller is already transferring the next record into buffer memory in anticipation of another Read from the Host. The Data Buffer and Drive Controller continue their sequence of Read-Completion Status until the buffer memory is full. Buffer memory won't fill up until the Host stops issuing Read commands to the drive.

The following is the process for an interface to data buffer, multi-record sequential Read (the most common tape drive operation).

1. Interface issues Read to Data Buffer
2. Data Buffer allows handshake of Read data from buffer memory to Host via Interface because data is already in the buffer memory
3. Data Buffer immediately issues Completion Status to the Interface when the transfer is done.
4. When Host sends next Read command, the process starts over with step #1.

5.2 Power Distribution System

There are two motor drive / power suplies in use; the 07980-6xx05 and the 88780-6xx05. The 88780-6xx05 supply is guaranteed to meet IEC 950 regulatory specifications as the result of a minor layout change. The 88780-6xx05 is used in all 88780A/B products.

Because of the early intro date of the 7980 Series of products, they do not need to meet the newer IEC 950 supply. The 07980-6xx05 is used in all 7979/7980/products.

Motor Drive / Power Supply

This supply provides pre-regulated 48 Volts at 6 amperes to power the Switching Motor Drive Amplifiers and to power the DC-to-DC Forward Converter which makes the System Power Supply (+5V at 11 amps,+12V and -12V at 1.5 amps). The 48V supply also powers the autoload blower fan, the cooling fan, and all solenoids used in the tape drive.

The supply can be operated with an AC input from 85 Vrms to 135 Vrms (for 120 VAC setting). (NOTE: The limits to this supply range apply to the power supply, not to the drive as a whole.) The control circuits for the 48V supply and also for the system power supply are operated from a +14V start-up supply (Vs). Two 6A fuses are on the Motor/Power PCA; F1 (nearest the casting) is for motor protection, F2 is for 48V system power (includes +5 V, +12 V, -12 V supplies).

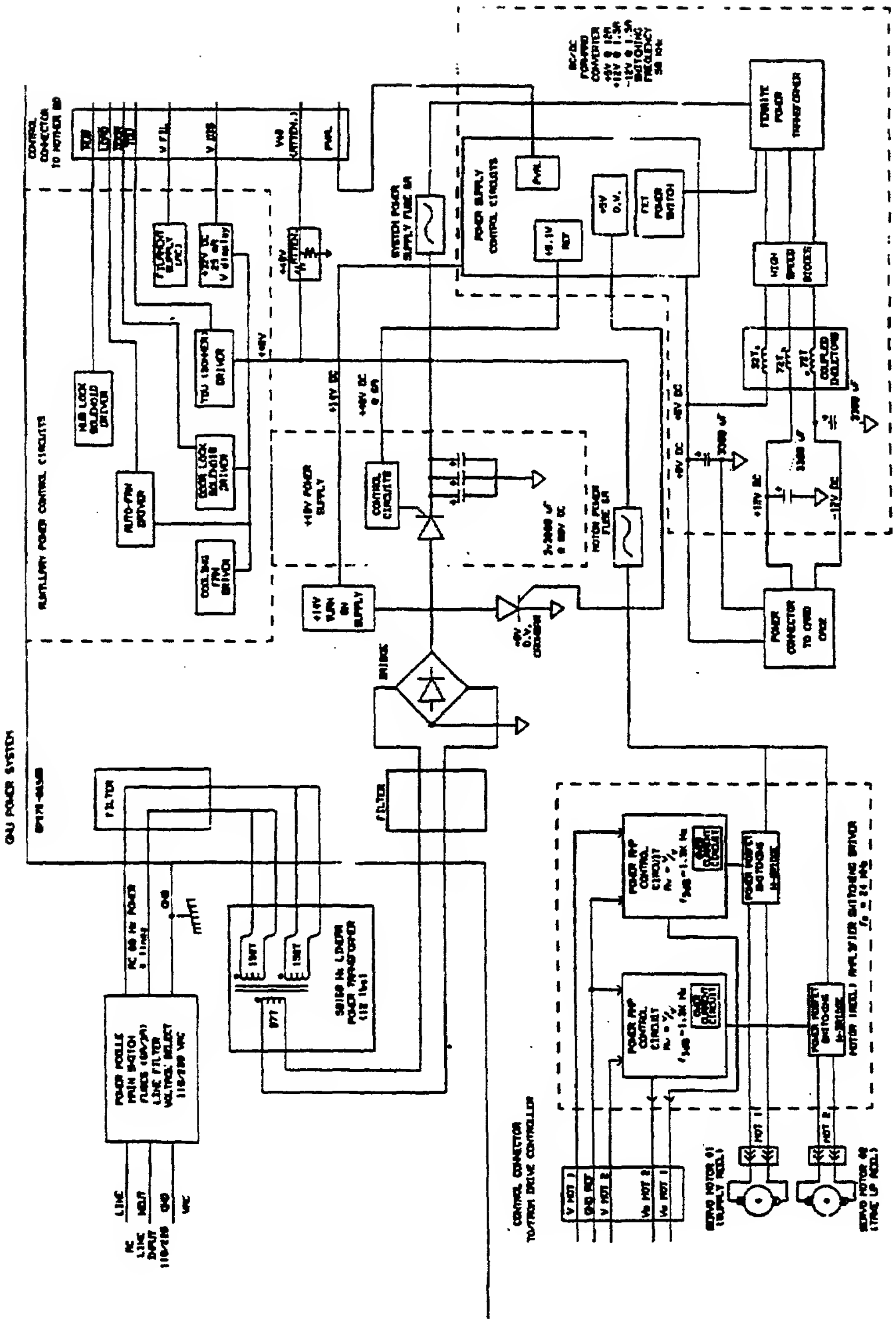

Figure 5-4. Power Distribution Block Diagram

System Power Supply +5, +12, -12

The function of the system power supply is to power the motor drive, the analog R/W system, the PLL system, the digital R/W formatters, the servo system controller and the interface/buffer circuits. The 12V supplies are held to a 10% value change as the 5V supply is changed from a no load to a full load condition.

Motor Drive Switching Amplifier

The Motor Drive Switching Amplifier provides power to the reel motors on command from the servo controller system. The driver has a voltage gain of 7 and a bandwidth (-3Db point) of 1.3 KHz.

Each motor driver amplifier is equipped with an overcurrent circuit which disables the drive circuit if the driver attempts to drive more than 6 amperes. A TTL-level signal, OVI1 or OVI2 (overcurrent motor 1 or overcurrent motor 2, respectively), is sent to the main controller to report the status of the overcurrent disable latch. Motor 1 is supply, Motor 2 is takeup.

Each motor driver circuit also sends an analog voltage back to the controller which is proportional to the voltage applied to the motor. This voltage is used to implement the variable speed rewind and is also used during motor drive circuit diagnostic testing.

Power Supply Specifications

Voltage	Tolerance	Ripple Voltage	Current
48 V	+/- 10 %	4 V max 120 Hz	8 A RMS
5.1 V	+/- 3 %	0.1 V max 50 KHz	11 A DC
12.5 V	+/- 10 %	0.2 V max 50 KHz	1.5 A DC
-12.5 V	+/- 10 %	0.2 V max 50 KHz	1.5 A DC

Motor Drive Voltage Amplifier Specifications		
DC gain	7	+/- 10 %
POLE	1.3 KHz	+/- 10 %
Switching Frequency	24 KHz	+/- 15 %

Power Good Specifications		
High Level Voltage	3.0 V min	5.0 V max
High Level Current		2.5 mA max
Low Level Voltage		0.5 V max
Low Level Current		10 mA max

5.3 Motion Control System

Servo Controller

The servo controller for the drive has three functions. It loads and unloads the reel and tape automatically, moves the tape under closed loop control of tension and velocity, and has diagnostic capabilities. The servo electronics do not have adjustments. Refer to the block diagram in Figure 5-5 for the following discussion.

Closed-Loop Operation

The control system for the drive consists of two relatively uncoupled servo loops. The tension loop senses tape displacement with a buffer arm and linear Hall effect sensor. The tension signal is processed by an analog feedback loop and fed to the supply reel. The velocity feedback is accomplished with an analog and digital hybrid loop. The output of this loop is fed to the takeup reel and also to the supply reel. Only feedback to the takeup reel is necessary; feedback to the supply reel is used to reduce the motion of the tension arm during ramping. Once the tape is loaded, the tape is always under closed loop control.

The velocity loop is a digital/analog hybrid to take advantage of the best features of each type of control. A position encoder is used by the drive controller to measure velocity. This is done by counting the number of pulses of the encoder every 5 ms. The encoder effectively has a resolution of 215.6 counts/inch tape. The velocity is compared with a velocity command at each sample period, and the error is accumulated over time. The resulting number is sent to a 12 bit D/A converter. This scheme performs the integral control operation with high accuracy. The reading of velocity is interrupt driven, but does not have to be of the highest priority; no counts are lost if the measurement is done with some delay, and only the integral of the error is sent to the loop.

The second part of the feedback is accomplished by a tachometer circuit which converts the pulses from the encoder to a voltage. This output is summed with the digital control output to formulate an integral plus proportional control scheme. The primary attributes of this scheme are zero steady state error, low sensitivity to variations, good phase margin, and low processor involvement.

The tension loop is completely analog. This is convenient because the output of the buffer arm Hall effect sensor is analog. The tension servo is best viewed as a correction servo on the primary velocity servo. The velocity servo feeds voltages to both motors which moves them roughly at the same angular velocity. If the reels both move at the same linear velocity, there is no need for tension arm motion. Since the reel radii vary over a 2:1 ratio as the tape travels from BOT to EOT, there is a difference between the angular speeds of the reels. The tension arm moves and commands the tension servo to take up the slack. The compensation of the tension loop also has an integral term to bring the tension arm to zero steady state error. The processor can disable the integration to assist in loading the tape.

Variable speed rewind is an important feature. It allows reduction of rewind time for a 2400 ft. reel from 120 seconds to 90 seconds. The maximum rewind speed attainable by a tape drive is mainly dependent on the voltage available to drive the motors. When either the supply or takeup reel is empty, the required voltage for a given speed is maximum. The servo always operates, even during rewind. The actual motor voltages are measured with the A/D converter and the velocity command is adjusted until all the available voltage is utilized. With a 48 volt supply, the maximum velocity is about 450 ips, and the average velocity is 320 ips.

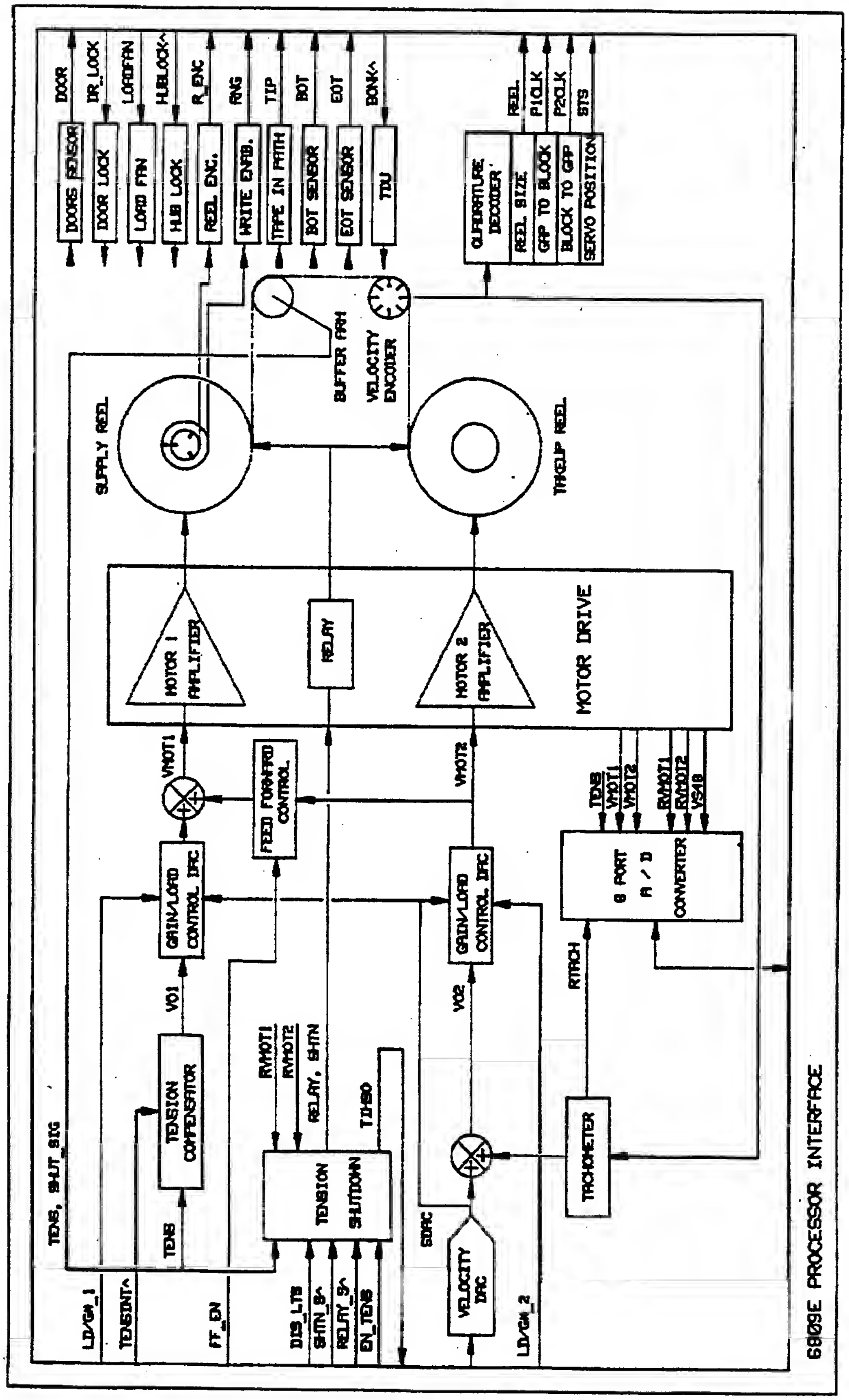

Figure 5-5. Servo Controller Block Diagram

The servo also has a number of auxiliary functions which improve its performance. A processor adjustable gain stage can independently adjust loop gains and provide better stability margin for different reel sizes. This circuit has a second function during autoload; it can individually drive each motor in an open loop mode. The tension arm has an optical switch which shuts the motor drive down immediately if the arm is out of range.

Autoload Operation

The autoload algorithm is described below. First, the proper operation path is explained, and then the possible error conditions and the response to each of these. The information collected for later use at each stage is also given. Each exception relates to one of the numbered proper operation steps above it. Motor 1 is the supply motor, and Motor 2 is the takeup motor.

A—Lock the Door and Detect Reel Presence

1. Poll the door sensor. After a power up or if the door changes from open to closed, start the autoload operations.
2. Check to see if the tape is threaded. Under some conditions such as a power fail recovery, the tape will already be threaded. To detect this condition, move the supply motor in the negative direction slowly while monitoring the velocity encoder and tension arm. Drive the takeup motor voltage to 0 volts. If activity is detected on these sensors , the tape is already threaded and autoload will proceed with locking the hub and closure of the servo loops.
3. Turn the load fan on.
4. Find a tape reel. Put both gain/load stages in the load mode. Move supply motor CCW slowly until reel encoder pulses are detected or a timeout occurs.
5. Reel seating check. As the reel rotates, check the time between successive reel encoder pulses. Compare these times against each other and against a standard to determine whether all the reel encoder pulses are there. If one or more of the encoder masks are missing then the times will be out of spec for a given rotational velocity of the motors.

6. Check for inverted reel. As motor rotates, monitor tape in path sensor. If tape is inverted, tape will continuously be detected within the timeout since tape is piling up in the tape path. If tape is stuck to the reel, tape will not be detected.

Exceptions/Response to Steps in 'A'

1. If timeout occurs, no reel was found. Autoload stops. The door remains closed.
2. No reel pulses are found or they do not match the timing requirements . The drive motor shakes the reel back and forth to attempt to seat it. Small reels sometimes require this operation. Repeat the reel find sequence up to 2 times. If this is unsuccessful, the load is aborted.
3. If tape is inverted, tape is drawn out of the tape path and the INVERT message is displayed.

B—Lock the Hub

1. Energize the hub lock solenoid. This keeps the hub from rotating and allows the supply motor to turn. the motor turns and locks the reel down with the three reel locking tabs The Fan is also turned on to help organize the tape.
2. Ramp the supply motor clockwise (CW) until the hub feet lock the reel in place or 25 volts is reached. The reel encoder does double duty and determines whether the locking operation was successful. When the feet are properly locked, the reel encoder interrupter is over the sensor. Since the hub may bounce on the hub lock arm, the motor is held in place after the reel encoder is detected for the first time, there is a 0.5 second wait for the reel to settle, followed by a second read to make sure that the reel is properly locked.
3. Release the hub solenoid. Motor 1 rotates counter clockwise (CCW) slowly and waits for the hub lock arm to drop out of the way. Motor 1 stops.
4. Measure the approximate reel size through an inertia measurement. This information can be used to provide the correct feed timeout for the thread tape operation. Motor 1 rotates CCW, slowly until a reel encoder pulse

is detected. A step voltage in the same direction is applied until the next reel encoder pulse is found. The time for this is related to the reel inertia.

Exceptions/Response to Steps in 'B'

1. It is very important to protect the hub from being accidentally damaged by the hub lock arm. The hub lock should never be energized while motor 1 is rotating. The black lever near the hub should not be pulled while the drive is in motion or the hub may be damaged. The present protection is to only access the hub lock bit by a routine which first commands an immediate 0 volts to the motors and then waits for the motors to stop. The required wait is 0.75 sec. This should drop the velocity of the motor to 5% of its original value before the hub lock is activated.

   The load operation is aborted if the hub lock is not successful, the reel encoder pulses are not found or if the hub solenoid fails to engage the hub lock arm. This error condition is detected if the hub lock voltage is applied and the hub continues to spin.

C—Thread the Tape

1. If a 7 inch reel is detected continue with step 2. Move the supply reel CCW and use the TIP sensor to identify the beginning of the tape leader. This is done by alternately waiting for no tape in the path and then tape in the path. This cycle is repeated twice and then aborted when no tape is detected. Motor 1 is then stopped and a delay used to allow the air to reorganize the tape. Motor 1 turns slowly CCW until the tape is out of the path. At this point the tape leader is pointed at the tape path entrance near the tension arm.

2. Move the supply reel forward (CW) slowly and the takeup reel more rapidly to thread the tape. A timeout is started at this point to indicate failure of the thread operation. The tape is slowly fed through the tape path to the takeup reel. The takeup reel is driven more rapidly to establish a rotating airflow around its hub. When the tape reaches the takeup reel, it winds itself around it and blocks the airflow to the load fan. Subsequent wraps firmly anchor the tape to the takeup reel. This condition is detected by monitoring a change in the position of the speed encoder. The encoder only turns once the tape starts wrapping itself around the takeup reel. The thread operation is complete when the

position measurement indicates that the takeup reel has two wraps or the timeout has elapsed.

3. Turn off the load fan.

Exceptions/Response to Steps in 'C'

1. If no tape in path is detected within the timeout, then the tape is stuck to the reel by static or sticky material. Motor 1 is accelerated quickly CCW to high velocity, and then slowed down to the tape finding speed to attempt to dislodge the tape. If it is not then the load is aborted.

   If during the above operation the tape is detected in the path continuously, the tape reel is assumed to be inverted since instead of drawing the tape leader across the tape in path sensor, the tape piles up in the tape path. In this case the load is aborted and the front panel displays "INVERTED".

2. Failure of this operation is indicated by expiration of the thread tape timeout before the takeup hub wrap is measured by the speed encoder. If this is the case, motor 2 is driven to 0 volts, and motor 1 withdraws tape until the tape in path sensor indicates no tape in path. The thread tape operation is re-tried from the start of Step 2 up to four times. If it still fails, then the load is aborted.

   The load is also aborted if the tape is not in the path for more than 1 second while threading it or if the supply motor fails to achieve the proper feed rate within a timeout.

D—Close the Servo Loops

1. Disable the low tension shutdown circuit.

2. Drive the motors in relative opposition to slowly tension the tape. Read the output of the tension arm with the A/D converter until it reaches roughly zero volts. As the tension arm passes the low tension shutdown limit, the low tension shutdown is re-enabled.

3. Change the tension loop gain/load stage to the gain mode and load the initial loop gain. Also set the integrator to the integrate mode. These operations bring the tension arm to the centered position. The drive waits for this loop to stabilize.

4. Change the velocity loop gain/load stage to the gain mode and load the initial loop gain. Allow the digital velocity loop to accumulate error. Now the servo is fully under closed loop control.

Exceptions/Response to Steps in 'D'

1. The tension should be established within a close loops timeout. If it is not, the tape may be improperly connected to the takeup hub. The Load is aborted in this case.

E—Find BOT

1. Move forward until the BOT Sensor is found.
2. Reposition the tape before the BOT and stop.

Unload

This routine assumes that BOT has been found, or that the starting tape position has been reached.

1. Disable the low tension shutdown. This is done to avoid a relay shutdown when the tape is drawn out of the path. The relay should only be actuated once when the machine is powered up or when an emergency occurs in the drive (such as a power failure).
2. Turn on the load fan. This helps to organize the loose tape when tension is lost.
3. Move the tape backwards until tension is lost.
4. Change the gain/load stages to the load mode.
5. Draw the tape out with motor 1 while monitoring the tape in path sensor until it is fully removed.

Unlock the Hub

1. Stop motor1.
2. Engage the hub lock solenoid.
3. Ramp motor 1 in the CW direction until the unlock voltage is reached.

4. Disengage the hub lock arm. Move motor1 CCW slightly so the arm will drop out, then stop the motor.

5. Turn the load fan off.

Unload/Abort

1. On unload commands from the front panel during load, flash unload on the front panel and withdraw the tape from the path immediately, then unlock the hub and open the door.

2. On abort load required by the above exceptions, send an error message to the front panel, open the door, and either accept further commands from the operator for recoverable conditions or ask the operator to open the drive.

Servo Subsystem Specifications

The following specifications are defined in terms of tape velocity.

Read/Write Speed

Nominal speed for GCR	123 ips
Nominal speed for PE	130 ips
Long term speed tolerance (dc component)	±1%
Short term speed tolerance (ac component)	±4%
Maximum rate of change	650 ips^2

Tension at Head

Nominal tension during read/write	10 oz
Tension rate of change	< 317 oz/s
During load, repositioning, and power failure	< 60 oz

Repositions

These times are best cases assuming GCR 0.28in Gaps and no time spent traveling over records (minimum record size).	
Access time (ramp to PE velocity and settle to 4%)[1]	360 ms
Reposition time (from PE velocity to same record)	1080 ms
Total Reposition time	1444 ms

1 These times are best cases assuming GCR 0.28in Gaps and no time spent traveling over records (minimum record size).

Rewind Time

Nominal time for 2400-ft reel	90 seconds
Nominal time for 3600-ft reel	135 seconds

Tape Requirements

Two types of tape will be supported:	
1.9 mil tape	Specified by ANSI X3.40-1976
1.3 mil tape	Nonstandard -0.1 mil +0.05[1]

1 The 7979A/7980A/7980XC/88780A drives accept "1-mil" tape. See statement in Chapter 1, "Specifications" for conditions of support.

Autoload Specifications

Percentage of complete autoloads	The drive will load tape correctly 98.5% of the time with 90% confidence.
Autoload time	Autoload will take less than 1 minute.
Autoload tape requirements	Autoload will work with 6, 7, 8, 8.5 and 10.5-inch reels with standard (1.9-mil ["2-mil"]) tapes and thin (1.3-mil ["1-mil"]) tapes.[1]

1 Smaller reels (6in and 7in) have a lower success rate than large reels. Also 1.3 mil ("1 mil") tapes have a lower autoload success rate. Some tape manufacturers recommend using 1.5 mil leader when using their 3600-ft tapes in autoload drives.

5.4 Drive Controller PCA

The Drive Controller is the overall controller for the servo, read/write electronics, phase locked loop, front panel, and the read and write formatters. The controller communicates to the outside world directly via the front panel, or indirectly via the host system through the data buffer and interface sections. All drive diagnostics are sequenced from the Drive Controller PCA.

Microprocessor/Timing

The microprocessor/timing portion of the Drive Controller contains ROM, RAM, System Clock generation, timer, and address decoding logic.

The processor is a Motorola 68B09E and operates at a 1.67MHz bus cycle. This speed was chosen because of the synchronization required between the controller and the read formatter circuitry. The main processor clock is the E_CLK. Another clock, Q_CLK, is also generated in quadrature to the E_CLK to aid in address decoding and bus synchronization.

The MC68B40 Programmable Timer Module generates the servo time slice waveform (2.5 ms).

Servo Registers

These registers serve as the communication link between the digital part of the Drive Controller and the analog (servo) electronics. The processor receives signals from the sensors and motors through these registers and communicates back to the servo system through the registers.

Position Capture

A position count is initialized and stored in this section when the tape is loaded and at BOT (more exactly, the Load Point). This number is incremented when each of the following five conditions occur:

- assertion of P1CLK—a gap to block boundary sensed
- assertion of P2CLK—a block to gap boundary sensed
- servo time slice interrupt
- reel encoder pulse (every 2.5 ms)
- READ_QDC line asserted by the microprocessor

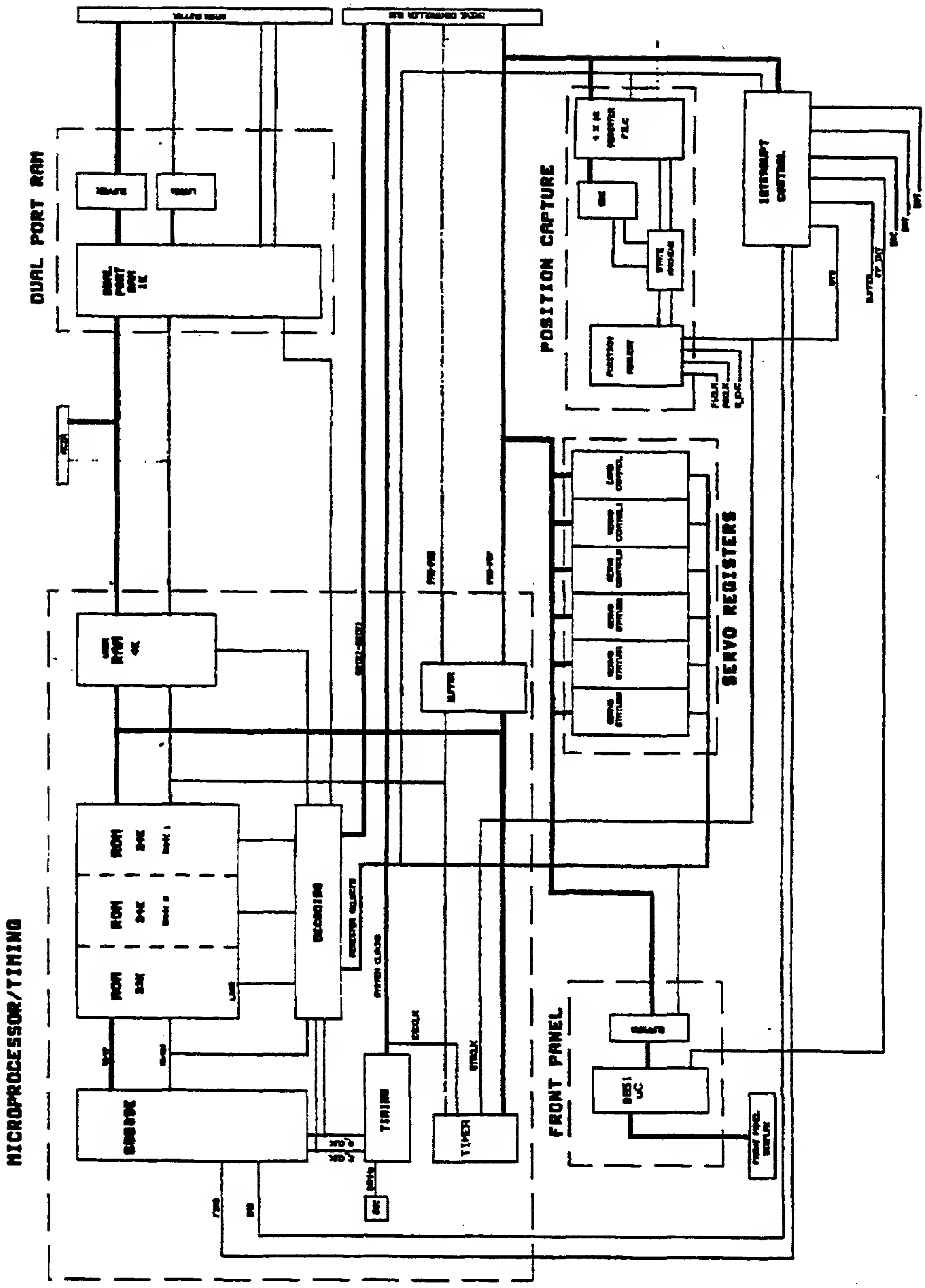

Figure 5-6. Drive Controller Block Diagram (Digital Section)

Dual-Port RAM

The Dual-Port RAM provides the communications link between the drive controller and the data buffer. Although normally polled, the Dual-Port RAM also provides an interrupt line to the processor. Address collisions are arbitrated by on board circuitry which sends a READY line back to the device which tries to access the same Dual-Port RAM location already being accessed by another device.

This 1Kx8 RAM is logically partitioned into areas for reception of messages, transmission of messages, and reports. A 'global' area in this RAM is set aside for shared information which both the Data Buffer and the Drive Controller can use. The software clock, which is generated every 50 ms by the Drive Controller, is stored in this global area.

Interrupt Control

This is the control for the Servo time slice interrupt. Every 2.5 ms the processor is interrupted to update the Dual-Port RAM, check for Speed Encoder Pulses, update the tape odometer, and other housekeeping functions.

Front Panel

The two-way communication between the microprocessor/timing block and the Front Panel is through an 8051 microprocessor and a buffer.

System Reset

A system reset line is provided by the drive controller to bring all the boards to a known state. This line is asserted by either a) PVALID de-asserting or b) a hard reset switch on the drive controller. The PVALID line is also available to those subsystems which require it directly.

Controller Bus

Within the unit, inter-board controller communications is through a controller bus which is resident on the mother board. The controller bus signal lines are detailed below.

Signal Definitions:

CLK_M	CLK_M is a 6.67 MHz non-interruptable master clock. This clock has a 66% duty cycle.
CLK_C	CLK_C is a 1.67 MHz non-interruptable clock. This clock has a 50% duty cycle.
CLK_E	CLK_E is a 1.67 MHz interruptable clock. This clock has a 50% duty cycle. When not interrupted, CLK_E is in phase with CLK_C.
CLK_Q	CLK_Q is a 1.67 MHz interruptable clock. This clock has a 50% duty cycle. When not interrupted, CLK_Q is in quadrature with CLK_C.
2XCCLK	2XCCLK is a 3.33 MHz , 50% duty cycle, non-interruptable clock used by the formatters and position capture subsystem. This clock is synchronous with CLK_C.
SS[3]-SS[5]	Subsystem select lines. These lines are active low.
SYSRESET	System reset line generated by the drive controller.

Write pulse.	Provides a rising edge to subsystems when 68B09E write data is valid.
PA[0]-PA[4]	Address lines. These lines are active high.
PD[0]-PD[7]	Data lines. These lines are active high.
R/W*	Read/write select line. A read bus-cycle is indicated by a logic high.
READY	Peripheral ready. This line is used to delay completion of the current bus-cycle. Completion of the current bus cycle is delayed when this line is asserted low. Peripherals that use this signal should use an open collector driver that can sink 10 mA.
PVALID	Power valid. When asserted high, power is good. De-assertion occurs 10 ms prior to loss of power.

5.5 Buffer PCA

There are two versions of the Buffer PCA. The original version, 07980-6xx04, is the standard, high-performance buffer found in early 7979A and 7980A. The second version is seen in the family of PCAs 07980-6xx14, 07980-6xx24, and 07980-6xx34.

Two differences between the older "04" PCA and the new family is surface mount technology and the use of a 68000 processor instead of a 68B09E. The 68000 is a faster, more powerful processor and its use decreases overhead time and enables data compression computations during transfer from the host (introduced in the 7980XC).

The 07980-6xx14 adds the capability of 800 NRZI. This PCA has been replaced by the 07980-60034. The 07980-6xx24 adds data compression, the 07980-6xx34 adds 1 Mbyte cache memory, and supports 800 NRZI.

Table 5-1. Data Buffer Matrix

PCA	Format				Buffer		Code Rev	Status
	XC	GCR	PE	NRZI	512K	1M		
07980-60004		X	X		X		3.XX	Last shipments 5-28-91 Support Use Only.
07980-60014		X	X	X	X		6.XX	Last shipment 4- 19-91 Replace with FRU 34.
07980-60024	X	X	X		X		6.XX	7980XC and 88780B Opt. 400 Only.
07980-60034		X	X	X		X	6.XX	For all non D.C. Units After 5-28-91.

The Buffer PCA processes all communications between the Interface and a Drive Unit. It accepts tape commands from the Interface, executes them, then responds with the resulting status. The Buffer communicates with the Drive Controller, sending it the command requests and receiving status information. Read and write data are transferred between the Interface and a Formatter through a large data buffer. The Buffer utilizes this buffer space to maintain streaming and to perform retries of failed operations.

A block diagram of the Buffer PCA is shown in Figure 5-7. The Buffer has three main subsystems. The controller subsystem contains a 68B09E microprocessor (04 PCA) or 68000 microprocessor (14, 24, 34 PCAs), 48K bytes of ROM, 8K bytes of non volatile RAM, 1K byte of Dual Port RAM, and the associated addressing and I/O circuitry. The data buffer subsystem contains the data buffer control circuitry and a 512K by 9 bit memory (1 Mb by 9 bit on the 34 PCA). The optional data compression subsystem contains the data compression control circuitry, data FIFOs, and the data compressor (data compression will not be discussed at this time).

The controller subsystem is responsible for the processing of command and status information between the Interface message bus and the Drive Controller message bus. It will setup and oversee data flow operations through the data compression and data buffer subsystems. The controller subsystem must maintain streaming and perform retries of failed operations.

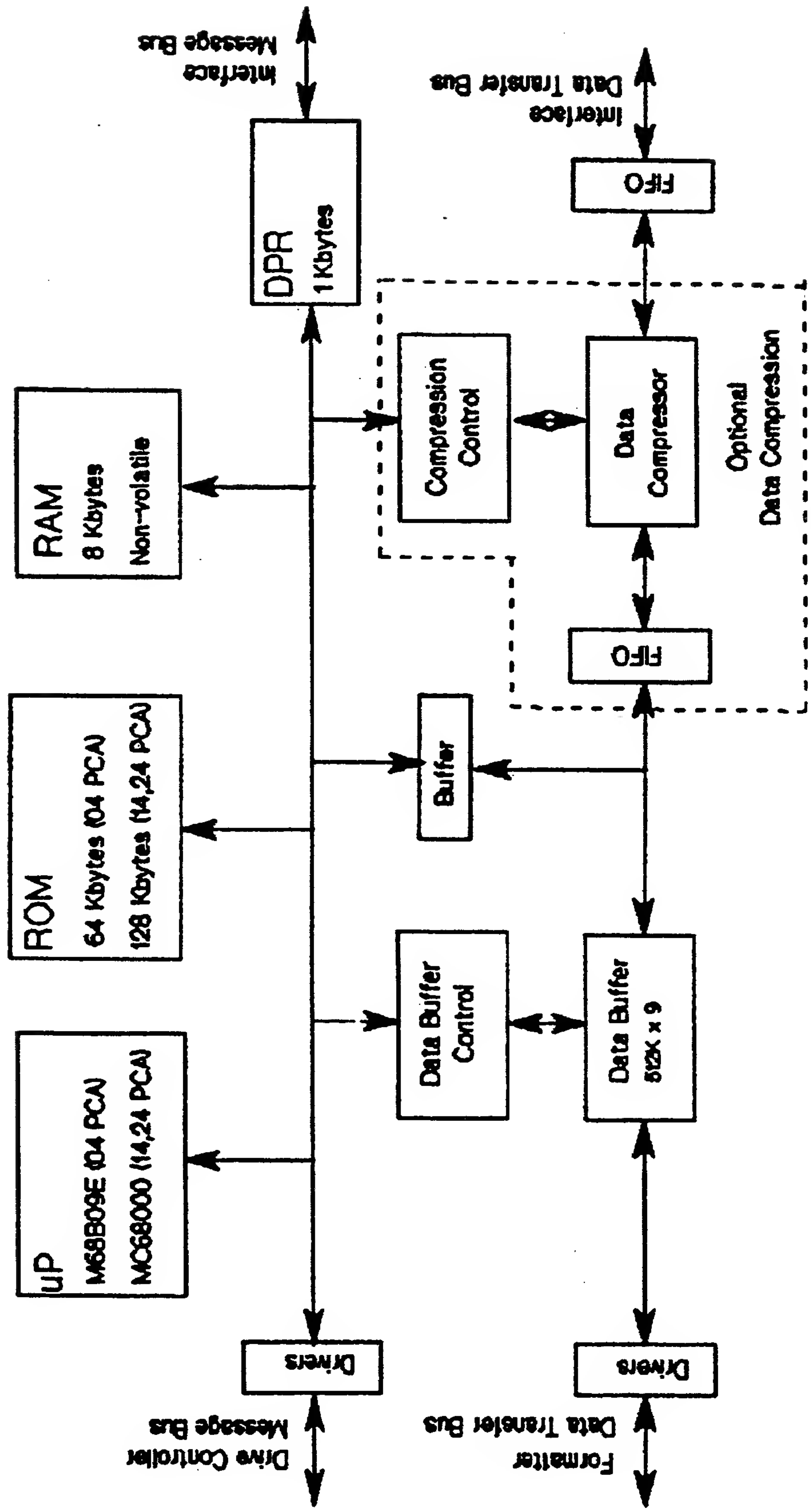

Figure 5-7. Buffer Block Diagram

The data buffer subsystem is responsible for the transfer and storage of data between the Interface data transfer bus and the Formatter data transfer bus. It is capable of simultaneously maintaining a 1.67 Mbytes/s transfer rate with an Interface and a 1.67 Mbytes/s transfer rate with a Formatter. The data buffer subsystem utilizes a starting address/length count memory accessing scheme. Data is accessed sequentially in a FIFO manner. A parity bit is received, checked, stored, and then sent with each data byte. An end-of-data bit is received and sent to flag the last byte of a data transfer.

Buffer Controller Subsystem

A general block diagram of the Data Buffer controller section is shown in Figure 5-8. The system consists of a Motorola 68B09E (or 68000) microprocessor, two 27256 32K (or 27512 64K) ROMs, a TC5564PL 8K x 8 CMOS RAM with battery backup, a 1K dual-port RAM, and supporting circuitry. The 68B09E and 27256 are used on the 04 PCA. 68000 & 27512 are used on 14, 24 and 34 PCAs.

Microprocessor

The data buffer operates under the control of a 68B09E or 68000 microprocessor. Communication occurs indirectly to the front panel through the drive controller and to the host system through the interface. The MC68B09E is an eight-bit microprocessor that includes several registers and multiple addressing modes, while the 68000 is a 16 bit Microprocessor.

Clock Generation

The main processor clock for the 68B09E and 68000 is called ECLK and operates at a frequency of 1.67 MHz. Another clock QCLK, is generated in quadrature (ie. it is 90 degrees out of phase with QCLK leading ECLK) to ECLK and operates at the same frequency. Both E and Q clocks are derived from the master clock, MCLK, which operates at a frequency of 6.67 MHz.

CMOS RAM

Non-volatile ram is provided to store configuration information, firmware updates, and information logging. The ram is a CMOS 8K x 8 static ram with a lithium battery for backup. The RAM is guaranteed a standby current equal

to or less than 1 microamp under normal conditions. This corresponds to a battery lifetime of approximately ten years.

Dual-Port RAM

The Dual-Port RAM provides the communication link between the data buffer and the interface. Another dual-port RAM resides on the drive controller that provides the link between the drive controller and the data buffer. An interrupt flag is provided to permit communication between the port and the subsystem.

Arbitration logic is provided to resolve any conflicts that may occur if the same memory location within the dual-port RAM is accessed at the same time. An arbitration signal, M/S* (master/ subordinate) is provided that divides access to the dual-port ram into two windows; one for the master side and the other for the subordinate. A request for dual-port ram access will be synchronized and is granted if it is made during the appropriate arbitration window. Otherwise, the requesting subsystem must wait until it is his turn.

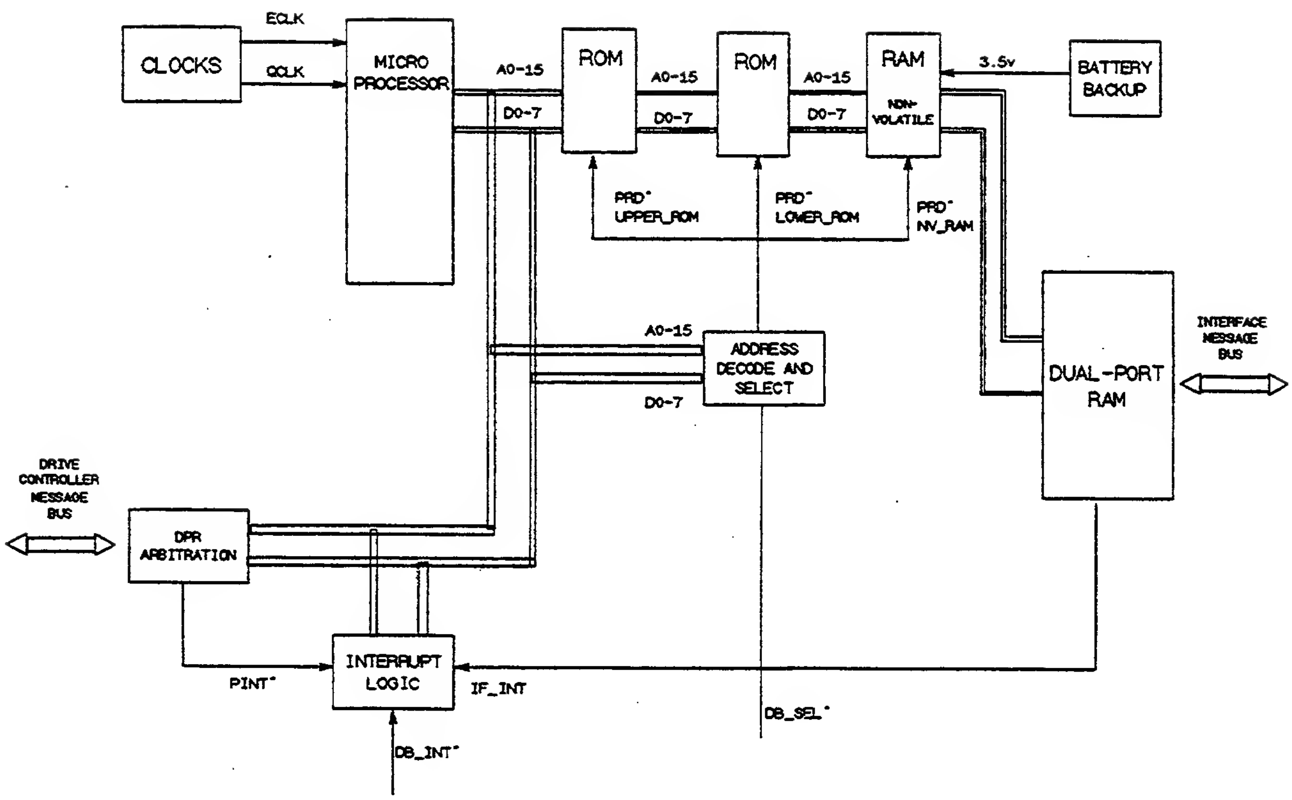

Figure 5-8. Data Buffer Controller Subsystem Block Diagram

Interrupts

The microprocessor supports 3 levels of interrupts; Non-Maskable (NMI), Fast interrupts (FIRQ), and standard Interrupts (IRQ).

NON-MASKABLE INTERRUPT

A non-maskable interrupt cannot be inhibited by the program and has a higher priority than FIRQ*, and IRQ*, and software interrupts. The entire machine state is saved when an NMI* occurs. An NMI* occurs when the clocks have been stretched by the RDY signal for a duration of 9 microseconds or greater.

FAST INTERRUPTS

Fast interrupts differ from standard interrupts in that they have a higher priority. They are faster because only the condition code register and the program counter are saved rather than the entire machine state. If more registers must be saved, this must be done through firmware.

The conditions that will cause a fast interrupt on the data buffer are either an interrupt from the from the device controller dual-port RAM or the interface dual-port RAM.

STANDARD INTERRUPT

The standard interrupt, IRQ*, has the lowest priority of the hardware interrupts and requires more time to service because it saves the entire machine state. A standard interrupt is caused only by the buffer memory subsystem.

Bus

The Bus provides the communication link between the data buffer and drive controller, and the data buffer and interface.

Data Buffer Subsystem

A block diagram of the data buffer subsystem of the Buffer PCA is shown in Figure 5-9. The data buffer subsystem is made up of six functional blocks. These functional blocks are: the master clock, the memory array, the data path, the I/O control, the address/length, and the transfer control. The master clock circuit generates all of the clocks for the data buffer subsystem as well as the main clock (6.67 MHz) for the controller subsystem. The memory array circuit contains a dynamic memory controller and a 512K by 9 or 1Mb by 9

memory array. It performs memory reads, writes, and refreshes at a rate 3.33 M cycles/s.

The data path circuit transfers data between peripheral systems and the memory array. It contains the data FIFO's for the Interface, the data transceivers for the Formatter, the data latches for the controller, and the data staging/pre-fetch latches for the memory array. The data path also performs parity checking of inbound data. The I/O control circuit interfaces the controller subsystem with the data buffer subsystem. It generates chip selects, read and write strobes, the buffer ready signal, and the buffer interrupt. The address/length circuit contains two 24 bit address pointers and two 24 bit length counters. This circuit increments an address pointer and decrements a length counter for each data byte transfer.

The transfer control circuit monitors the transfer request signals then oversees the transfer of data between peripheral systems and the memory.

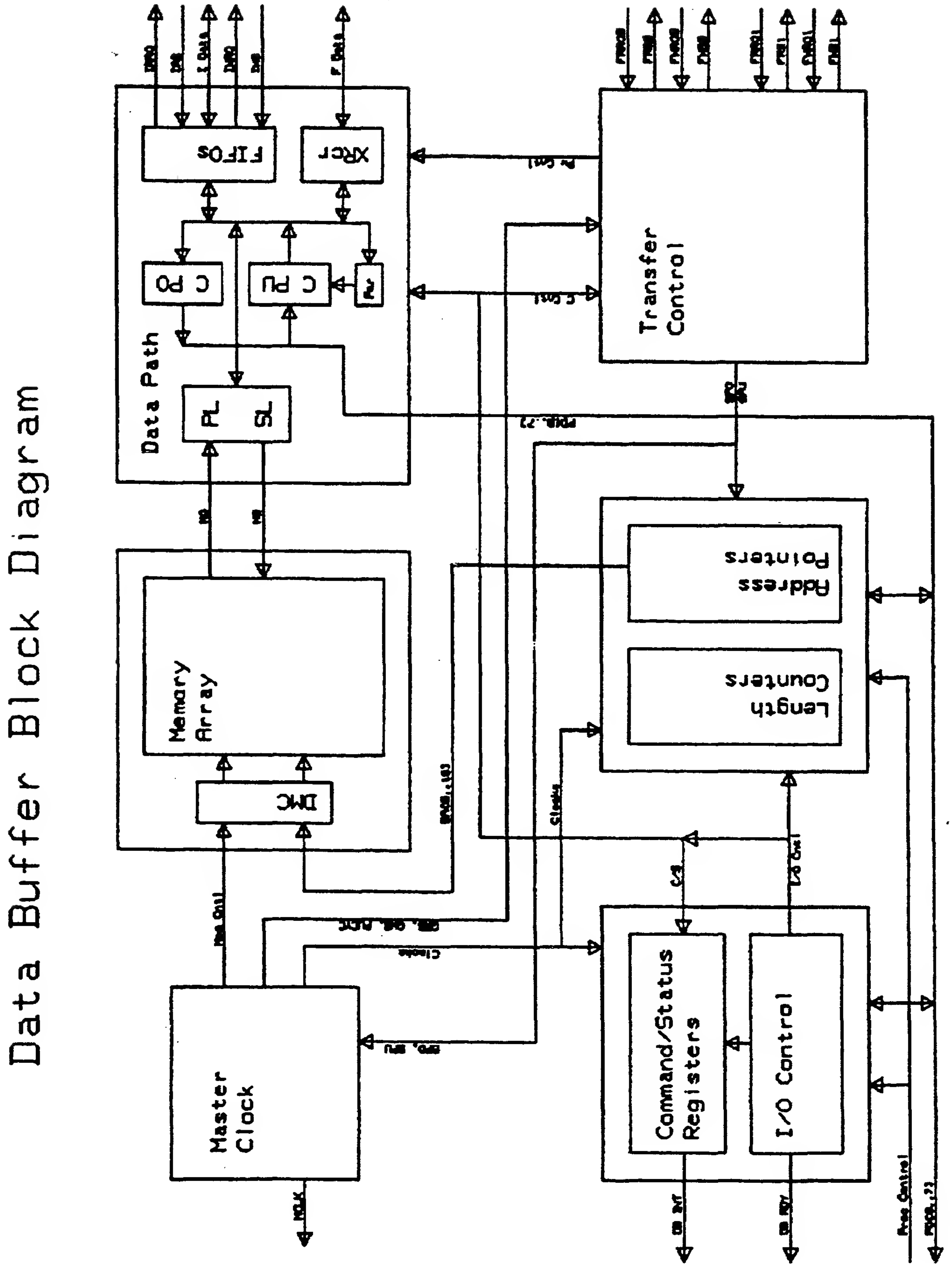

Figure 5-9. Data Buffer Subsystem Block Diagram

Master Clock

The master clock circuit generates all of the clocks for the data buffer subsystem as well as the main clock (6.67 MHz) for the controller subsystem. The master clock circuit primarily utilizes a 5 tap 150 ns delay line and some external logic.

The master clock circuit receives three control signals and generates four clocks, two generic transfer strobes, two write strobes, three address strobes, and two memory control signals. A timing diagram of the master clock signals is shown in Figure 5-2. The three control signals are PVAL, SPO, and SPU. PVAL is used at power up to indicate that power is valid and to initiate oscillations within the delay line.

SPO is used to select a memory POP cycle. SPU is used to select a memory PUSH cycle. The four clock signals are MCLK, BCLK, UCLK, and PUCYC. MCLK is the 6.67 MHz main system clock for the controller subsystem. It is also used by the data buffer subsystem for I/O control. BCLK is the input to the delay line and is a 3.33 MHz signal.

Each UCLK cycle represents one data byte transfer to memory and/or a peripheral system. UCLK is also the 3.33 MHz USM clock. PUCYC is a 1.67 MHz PUSH cycle clock. PUSH memory cycles occur during the UCLK cycle that PUCYC is high. POP memory cycles occur during the UCLK cycle the PUCYC is low. SELPOA is the invert of PUCYC. POP addresses are selected at the buffer USM when this signal is high. PUSH addresses are selected when SELPOA is low.

The two generic transfer strobes are GRS and GWS. GRS is the generic read strobe. It is qualified then sent to control output enables for the driving of a data bus during a peripheral data transfer. GRS is active for the last two thirds of a BCLK cycle. GWS is the generic write strobe. It is qualified then sent to control latch enables or register clocks for the capturing of data off of a data bus. GWS is active for one third of a BCLK cycle embedded within GRS.

The two write strobes are MLWS and LMWS. MLWS is the memory to latch write strobe. MLWS clocks data from the memory array to the pre-fetch latch. LMWS is the latch to memory write strobe. LMWS strobes data from the data staging latch into the memory array.

The four memory address strobes are MSEL, RASI, CASI, and LE. These strobes are used by the dynamic memory controller to perform memory reads

and writes. LE is the latch enable signal. It latches the 19 bit memory address into the dynamic memory controller. MSEL selects the row or column address output to the RAM array. RASI is the control input to the dynamic memory controller for the row address strobe which is sent to the RAM array. CASI is the control input to the dynamic memory controller for the column address strobe which is sent to the RAM array.

The two memory control signals are MC1 and MC0. These signals are sent to the dynamic memory controller as mode commands. Three mode commands are used, they are: Refresh, Read/Write, and Clear Refresh Counter.

Memory Array

The memory array circuit contains a dynamic memory controller and a 512K X 9 bit (1Mb by 9 bit on the 34 PCA) memory array. It performs memory reads, writes, and refreshes at a rate 3.33 M cycles/s. Control signals are received from the master clock circuit. A 19 bit address (20 bit address on the 34 PCA) is obtained from the address/length circuit. Data is read into the memory array from the data staging latch of the data path circuit. Data is written to the pre-fetch latch of the data path circuit.

There are two 9 bit banks of 256K bit memory chips in the RAM memory array (one 9 bit bank of 1Mbit memory on the 34 PCA). Each dynamic memory chip receives two address strobes, a write enable, and a 9 bit multiplexed address. Write data is received on one 9 bit bus while read data is sent on another 9 bit bus.

The control signals from the master clock circuit are MC0, MC1, MSEL, RASI, CASI, LE, MLWS, and LMWS. These signals are described above with the master clock circuit.

The 19 (20) bit address from the address/length circuit represents the memory location that data will be read from or written to. For more details see the address/length circuit description below. Data is transferred to and from the data path circuit. The data staging latch is used for all read data. The pre-fetch latch is used for all write data.

Data Path

The data path circuit on the Buffer Controller PCA, shown in Figure 5-7, transfers data between peripheral systems and the memory array. It contains

the data FIFOs for the Interface, the data transceiver for the Formatter, the data latches for the controller, and the data staging /pre-fetch latches for the memory array. The data path also performs parity checking of inbound and outbound data. The Interface data FIFO section contains an inbound FIFO of 16 words each 10 bits wide and an outbound FIFO of 16 words each 10 bits wide. Data is transferred to and from the Interface on ID[0..7], IPAR, and IEOD. These signals are an eight bit data bus, a parity signal, and an end of data signal. The Interface is sent the Interface write request (IWRQ) signal which is active when there is room in the inbound FIFO. The Interface will then drive the Interface write strobe (IWS) to clock data into this FIFO. The Interface is also sent the Interface read request (IRRQ) signal which is active when data is available in the outbound FIFO. The Interface will then drive the Interface read strobe (IRS) to receive the data. Three signals control the buffer side of the inbound FIFO. They are JRRQ, JRS, and PUCLR. JRRQ is the FIFO read request. JRS is the FIFO read strobe. PUCLR will clear the inbound FIFO. Three signals control the buffer side of the outbound FIFO. They are JWRQ, JWS, and POCLR. JWRQ is the FIFO write request. JWS is the FIFO write strobe. POCLR will clear the outbound FIFO.

The data transceiver for the Formatter will either receive or send data on the formatter data transfer bus. The formatter data transfer bus is an eight bit data bus (FD[0..7]), a parity signal (FPAR), and an end of data signal (FEOD). Two signals control the transceiver. FLRS drives the data from the formatter bus onto the internal buffer latch bus. LFRS drives the data from the internal buffer latch bus onto the formatter bus. These signals are qualified read strobes generated by the transfer control circuit.

The data latches for the controller enable the controller to read and write memory data. The controller write strobe (CWS) is used to latch POP data going to the controller. The controller can then read this data with the use of the buffer data read strobe (BDATRS) and the buffer extend read strobe (BEXTRS). BDATRS will strobe the data byte onto the processor bus. BEXTRS will strobe the parity bit and end of data flag onto the processor data bus. The controller can also send PUSH data to the buffer. It should first write the parity bit and end of data flag to the PUSH extend register with use of the buffer extend write strobe (BEXTWS). Then when it writes to the PUSH data register the controller read strobe (CRS) will transfer the controller's data to the data staging latch. The controller may alternatively make use of automatic parity generation as described below.

The data staging/pre-fetch latches hold all data read from or written to the memory array for one buffer clock cycle. The data staging latch is used for PUSH data. It is clocked by the latch write strobe (LWS). Nine bits of data are sent to the memory array while the tenth bit, the EOD flag, is sent to the transfer control and I/O control circuits.

The pre-fetch latch is used for POP data. It is clocked by the memory to latch write strobe (MLWS). Nine bits of data are received from the memory array while the tenth bit, the EOD flag, is received from transfer control circuitry and qualified by the end of write enable (EWEN) signal from the I/O control circuitry.

Parity checking is performed on inbound and outbound data. The parity circuit receives the control signal generate parity (GENPAR). When GENPAR is disabled the parity error signal (PERR) will indicate bad parity on data. PERR is sent to the I/O control circuit. When GENPAR is enabled the parity of data is computed and sent to the controller's PUSH extend register. The controller can use the parity generator when writing data to the buffer by setting the parity bit of the PUSH extend register to zero and GENPAR to one. Each byte written to the PUSH data register will then be sent to the memory array with correct parity.

I/O Control

The I/O control circuit interfaces the controller subsystem with the data buffer subsystem. It generates chip selects, read and write strobes, the buffer ready signal, and the buffer interrupt. The I/O control circuit also contains two buffer control registers and the buffer status register.

The I/O control circuit receives ten control signals from the controller subsystem. Two of these control signals are the processor's clocks PECLK and PQCLK. These clocks are synchronized to MCLK which is generated by the master clock circuit. Processor read and write cycles are distinguished by the read/write (PR/W*) signal. The data buffer subsystem is selected for an I/O transfer by the data buffer select (DB_SEL) signal. Register addressing is handled through the use of five address lines (PA[0..4]). The SYSRESET signal is used at power up to initialize all data buffer circuitry.

Data is transferred to and from the controller subsystem over the processor data bus (PD[0..7]). The controller will stretch I/O cycles until the data buffer requests the completion of a transfer with the data buffer ready (DB_RDY)

signal. The IOCNTL FPAL generates this ready signal. The data buffer can interrupt the controller at the end of data transfers either into or out of the buffer. The data buffer interrupt (DB_INT) signal is used for these interrupts. The I/O control circuit divides the data buffer register space in half. The lower half is used for buffer access, control, and status registers. The upper half is used for access to address pointers and length counters.

Address/Length

The address/length circuit contains two 24 bit address pointers and two 24 bit length counters. This circuit increments an address pointer and decrements a length counter for each data byte transfer.

Transfer Control

The transfer control circuit monitors the transfer request signals, and then oversees the transfer of data between peripheral systems and the memory array.

Data is transferred in two buffer cycles. One cycle is used to transfer data between a peripheral system and the data staging/pre-fetch latches. Another cycle is used to transfer data between the data staging/pre-fetch latches and memory.

The transfer control circuit receives read and write transfer requests from the interface FIFO's, the Formatters, and the controller. The transfer control circuit also controls the transfer of data between the data staging/pre-fetch latches and memory.

5.6 Formatter PCA

In older units the Read Formatter was located in the outermost slot (#4) in the cardcage.

After serial number prefix 2805A in the 7979A and 2806A in the 7980A, the functions of this PCA were placed on the Read/Write/PLL PCA (formerly 07980-6xx01) and only three PCAs were left in the cardcage. The new PCA (in slot #1) then became a Read/Write/Formatter/PLL PCA and the number of the PCA changed to 07980-6xx21 and is now 88780-6xx21. If the drive is configured to use 800 NRZI, this PCA is a 07980-6xx31. The Formatter decodes flux data from the tape into user data to be sent to the host computer. The operation of the Formatter is managed by software running on the Drive Controller. The Drive Controller oversees the reading of each block on the tape by setting up the Formatter, sending it a command to read, and then monitoring its status. The Formatter is capable of reading both 1600 cpi Phase Encoded and 6250 cpi Group-Coded Recording ANSI formats. Within these formats data records, tape marks, and ID bursts are written on the tape. The Formatter detects the presence of these blocks, identifies them, decodes the data, and corrects errors. The Formatter receives nine tracks of synchronized flux data from the Phase Lock Loop portion of the Read Electronics. The flux data is converted to binary data, and deskewed into nine bit words. These words are then decoded into user data after error correction. The user data is sent to the Data Buffer. The location and identity of each block on the tape is reported to the Drive Controller so that it can manage tape positioning. Error status for each block is also sent to the Drive Controller. Figure 5-10 shows a block diagram of the Formatter.

The Formatter contains two subsystems. These subsystems are the Data Detect and Deskew subsystem and the Read Formatter subsystem. The Data Detect and Deskew (DDD) subsystem contains the Read FIFO, the Slave Deskew, the Master Deskew, the Block Detect, and the DDD Command & Status blocks. The Read Formatter subsystem contains the Read Chip, the Data Buffer Interface, the Read Formatter Controller, the Byte Counter, the Read Formatter Command, and the Read Formatter Status.

Following the diagram are descriptions of each subsystem and the blocks which make it up. These subsystems and blocks are described by their function, inputs, process, and outputs.

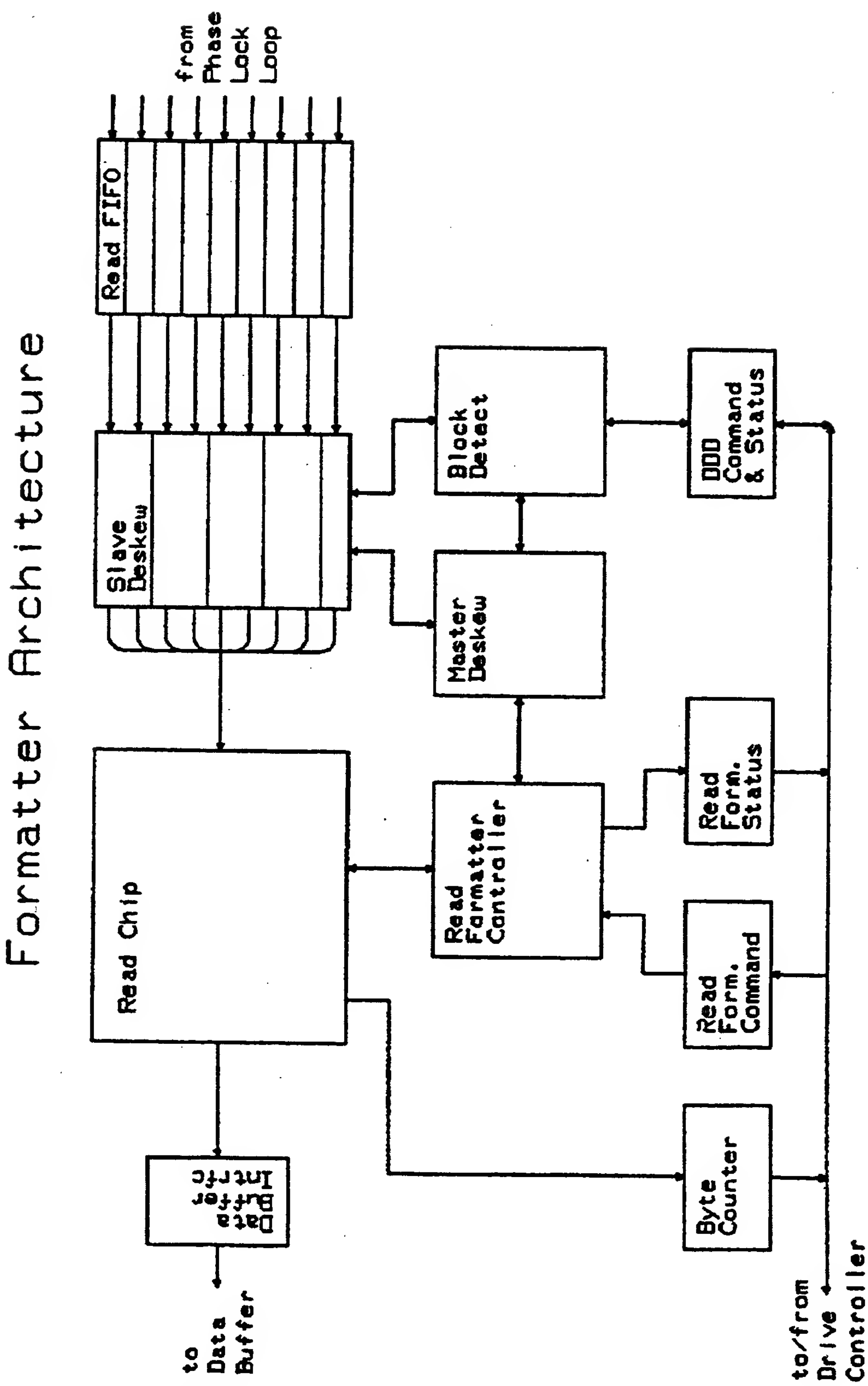

Figure 5-10. Formatter Block Diagram

Data Detect and Deskew

Function:

Convert nine tracks of flux data from the Phase Lock Loop into a deskewed binary word for the Read Formatter. Detect and verify block types read from the tape.

Process:

Receive setup and acknowledge commands from the Drive Controller. Receive flux data from Phase Lock Loop, convert this flux data into binary data through the use of either phase or NRZI decoding. Detect track in errors via bad flux code or the out of lock condition. Deskew the nine tracks of data into one word through the establishment of the best sync of all tracks. Send deskewed data to the Read Formatter along with track in error signals. Detect blocks and gaps, then determine block type. Verify non data blocks such as tape marks and IDs. Report block detection status to the Drive Controller.

Read FIFO

Function:

Receive and buffer flux data from the nine individual tracks prior to deskewing.

Process:

Accept flux data from Phase Lock Loop as made available. Buffer up to 25 bits of data per track for deskewing. Provide indication of flux data ready. Send flux data synchronously to the Slave Deskew. Provide the following four operating modes: 1) Forward flux data during search for sync mark, 2) Hold flux data during deskewing process, 3) Forward flux data during read, and 4) Serially flush flux data during error recovery. Provide indication of flux data forwarding.

Slave Deskew

Function:

Convert flux data from the Read FIFO to binary data. Detect track activity and error conditions. Detect and signal track synchronization.

Process:

Obtain flux data from Read FIFO when available. Convert this flux data into binary data through the use of either phase or NRZI decoding. Detect track in error by checking for bad flux code or an out of lock condition. Provide indication of track activity for the purpose of block detection. Search for track sync mark. Hold data in Read FIFO until deskewing is accomplished by the Master Deskew chip. Forward data and track in error information to Read Formatter. Detect and signal the track synced condition while data is read. Flush Read FIFO when out of lock or failure to sync.

Master Deskew

Function:

Control the nine Slave Deskew circuits to establish alignment of the skewed data.

Process:

Monitor the track sync signals from the nine Slave Deskew circuits. Measure distance from first track sync to ensure that the maximum skew is not exceeded. Establish the best track synchronization then signal all Slave Deskew circuits to forward their data to the Read Formatter.

Block Detect

Function:

Perform detection of the blocks which are recorded on the tape. Correctly identify and verify block type. Accurately locate and measure, blocks and gaps.

Process:

Monitor the track activity signals from the Slave Deskew circuits. Filter these signals such that gap noise and small dropouts within blocks are ignored. Detect the presence of a recorded block and signal the gap to block boundary. Identify the block type. Verify that this identification is correct. On read after write, verify that the recorded pattern of non data blocks meets ANSI standards. Monitor track sync and end of data signals in order to qualify data blocks and detect a gap before end of data condition.

Additional explanation of Block Detect is in "Block Detect Architecture" under the following subsection, "Block Detect Specifications."

Data Detect and Deskew Command & Status

Function:

Interface with the Drive Controller by accepting Data Detect and Deskew (DDD) commands and returning DDD status.

Process:

Accept and latch DDD commands from the Drive Controller. Provide appropriate control signals to the separate DDD circuits in performing the command. Accept and latch status signals from the separate DDD circuits. Return the DDD status to the Drive Controller. Facilitate handshaking of I/O with the Drive Controller at both the hardware and software levels.

Read Formatter

Function:

Decode the read data from Data Detect and Deskew. Utilizing the track in error signals, detect and correct errors.

Data Buffer

Function:

Read Transfer Acknowledge

Process:

Accept setup and acknowledge commands from the Drive Controller. Receive deskewed data along with track in error signals from the Data Detect and Deskew. Detect the start of each data field. If reading a GCR tape, convert each group of 5 characters to 4 characters. Detect data read errors and correct. Send corrected data with parity and end of data flag to the High Speed Data Link. Determine status of each data block and report it along with a count of the record length to the Drive Controller.

Read Chip

Function: Decode read data from the Data Detect and Deskew. Detect and correct errors.

Process:

Receive read data from the Data Detect and Deskew. If reading a GCR tape, convert each group of 5 characters to 4 characters. Detect data read errors and correct using the full capabilities of the recording format. Determine status of each data block.

Data Buffer Interface

Function:

Send read data to the High Speed Data Link.

Process: Request a data transfer, transfer data to the High Speed Data Link, verify that the transfer is complete.

Read Formatter Controller

Function:

Control the functioning of the Read Chip as each data record is read.

Process:

Detect the start of each data field, enable CRC calculation with the first data character. Provide sequencing control to the Read Chip for each GCR data group. Detect the end of block, signal it, and provide processing control to the Read Chip.

Read Formatter Command

Function:

Receive Read Formatter commands from the Drive Controller. **Process:**

Accept and latch Read Formatter commands from the Drive Controller. Provide appropriate control signals to the other Read Formatter circuits.

Read Formatter Status

Function:

Send Read Formatter status to the Drive Controller.

Process:

Obtain and latch status signals from the Read Chip and Read Formatter Controller. Return this status to the Drive Controller.

Byte Count

Function:

Provide a count of the number of bytes within a data record.

Process:

Count each character read by the Read Chip. Send this count to the Drive Controller upon request.

Block Detect Specifications

The Block Detect circuitry of the Formatter performs detection of the blocks which are recorded on the tape. It identifies and verifies block types. It also provides the Drive Controller/Servo system with a means to accurately locate and measure, blocks and gaps.

This Block Detect Specification contains six parts:

- block/gap detection
- block type recognition
- block verification
- block detect architecture
- drive controller interface
- block detect state machine

Block/Gap Detection

In performing block detection the Block Detect circuitry filters out noise, thereby eliminating unnecessary retries and avoiding false hard errors.

Positioning clock are sent to the Servo system at block to gap boundaries and a DATABAR signal is sent to the Read Formatter.

Filter main Gap signal to ignore drop-ins of less than 1/3 of smallest block along with full width dropouts of less than 1/3 of smallest block.

Provide Positioning Clocks for Servo. Provide two positioning clock signals to the Servo for gap to block and block to gap position referencing.

Provide DATABAR Signal for Read Formatter When entering a GCR block, DATABAR will change from 1 to 0 after 68 consecutive flux spacings of any track activity. This threshold was chosen because it is just larger than 1/3 of the minimum block size.

When exiting a GCR block, DATABAR will change from 0 to 1 after 68 consecutive flux spacings of no track activity. This threshold was chosen because it is just larger than 1/3 of the minimum block size and also larger than the Read Formatter pipeline for detecting Gap before EOD.

When entering a PE block, DATABAR will change from 1 to 0 after 22 consecutive flux spacings of any track activity. This threshold was chosen because it is just larger than 1/3 of the minimum block size.

When exiting a PE block, DATABAR will change from 0 to 1 after 44 consecutive flux spacings of no track activity. This threshold was chosen because it is just larger than 1/3 of the minimum block size and also larger than the Read Formatter pipeline for detecting Gap before EOD.

Block Type Recognition

In performing block type recognition the Block Detect circuitry must distinguish between data blocks, tape marks, density IDs, and noise. This function is done on a best-fit basis with some ability to ignore drop-ins, dropouts, and dead tracks.

Data Block. The sync OK signal (SOK) from Master Deskew is used for data block detection.

Tape Mark. A count of 32 (PE) or 128 (GCR) in the tape mark detect counter. This counter counts up flux spaces which look like tape marks, counts down flux spaces which look like data blocks or IDs, and ignores other activities and gaps. In GCR, activity in at least 5 of tracks 1, 2, 4, 5, 7, and 8 with erasure in tracks 3, 6, and 9 will increment the tape mark detect counter.

In PE, activity in at least 2 of tracks 2, 5, and 8 with erasure in tracks 3, 6, and 9 will increment the tape mark detect counter.

Activity patterns looking like an ID or a data block (activity in 8 of the 9 tracks) will decrement the tape mark detect counter.

Other activity patterns including gaps do not effect the tape mark detect counter. The tape mark detect counter will not decrement below zero nor change once the detect count has been reached.

Other Blocks.

GCR ID	There are 32 consecutive flux spaces of activity in track 6 with erasure in tracks 1, 2, 3, 4, 5, 7, 8 and 9. ARA Burst/Data: In read mode, 32 consecutive flux spaces of activity in at least 8 out of 9 tracks. In verify mode, 32 consecutive flux spaces of activity in all 9 tracks.
ARA ID	In read mode, 32 consecutive flux spaces of activity in at least 5 of tracks 2, 3, 5, 6, 7, and 9 with erasure in tracks 1, 4, and 7. In verify mode, 32 consecutive flux spaces of activity in tracks 2, 3, 5, 6, 7, and 9 with erasure in tracks 1, 4, and 7.
PE	There are 32 consecutive flux spaces of activity in track 4 with erasure in tracks 1, 2, 3, 5, 6, 7, 8 and 9.
Unknown	In PE, 16 consecutive flux spaces of activity not meeting one of the above pattern requirements. In GCR, 32 consecutive flux spaces of activity not meeting one of the above pattern requirements.
Noise	Activity of less than the maximum tape mark (PE: 256 flux spaces; GCR: 400 flux spaces) if not recognized as either a tape mark (TMDET), or data block (SOK) unless this activity is followed by a minimum length gap (0.25 inch).

Block Verification

The writing of gaps and non-data blocks must be verified. These blocks include tape marks, density IDs, and ARAs. The block verify circuitry will also be used in Read ID to identify the density of the tape.

Erasure in all tracks, meeting the following number of consecutive flux spaces.

PE:	320 fs	0.100 in
GCR:	1000 fs	0.111 in

PE ID — Activity in track 4 with erasure in tracks 1, 2, 3, 5, 6, 7, 8 and 9, meeting the following number of consecutive flux spaces.

32 fs	0.020 in	1600 frpi
104 fs	0.065 in	1600 frpi
200 fs	0.125 in	1600 frpi

GCR ID — Activity in track 6 with erasure in tracks 1, 2, 3, 4, 5, 7, 8 and 9, meeting the following number of consecutive flux spaces.

32 fs	0.011 in	3014 frpi
200 fs	0.066 in	3014 frpi
400 fs	0.133 in	3014 frpi

Block Detect Architecture

The Block Detect circuitry performs detection of the blocks which are recorded on the tape. It identifies and verifies block types. It also provides the Drive Controller/Servo system with a means to accurately locate and measure blocks and gaps.

The Drive Controller controls the Block Detect circuitry with setups and commands. The Deskew circuitry provides track activity information and a flux spacing strobe. The Read Formatter provides data record read status. The Block Detect circuitry uses these inputs to generate for the Drive Controller tape positioning clocks, block detect flags, and block verification status.

The Block Detect circuitry is made up of 8 functional blocks. These blocks are named, pattern decode, tape mark detect, gap filter, block/gap length, verify count, block read/verify, detect state machine, and command/status.

Pattern Decode. The pattern decode circuit determines the type of track activity currently being read from the tape. The pattern decode circuit utilizes the track activity signals (TA[1..9]) from the Deskew circuitry to generate detect type (DT[0..1]) for the tape mark detect circuit, gap (DGAP) for the gap filter circuit, and block type (BT[0..2]) for the verify count and block read/verify circuits. The mapping of the track activity signals to these output signals is performed by the pattern decode ROM.

Tape Mark Detect. The tape mark detect circuit determines if the block currently being read from the tape is a tape mark. The tape mark detect circuit utilizes the detect type signals (DT[0..1]) from the pattern decode circuit along with the flux spacing strobe from the Deskew circuitry. The tape mark detect circuit counts up flux spaces which match that of a tape mark while counting down flux spaces which match those of an ID or a data block. Flux spaces which are gap or unrecognizable are ignored. When a density dependent count threshold is met the tape mark detect signal (TMDET) is asserted for the detect state machine circuit.

Gap Filter. The gap filter circuit determines if either a block or a gap is currently being read from the tape. The gap filter is also responsible for generating the tape positioning clock for the Drive Controller/Servo. The gap filter receives the raw gap signal (DGAP) from the pattern decode circuit. The raw gap signal is filtered by counting up consecutive flux spaces either as gap or as block. When a density dependent threshold is met the not data signal (DATA*) is toggled appropriately. The gap filter also receives the current detect state (DSTATE[5..7]) from the detect state machine. The filtered gap signal is used along with the detect state to provide two tape positioning clocks (P1CLK and P2CLK).

Block/Gap Length. The block/gap length circuit measures the length of the block or gap currently being read from the tape. The block/gap length circuit receives the filtered gap signal from the gap filter circuit and counts consecutive flux spaces to determine the block or gap length (BGLEN[0..2]) for the detect state machine.

Verify Count. The verify count circuit validates IDs and tape marks written on the tape. The verify count circuit receives the current block type (BT[0..2]) from the pattern decode circuit and counts consecutive flux spaces to determine the verify level (VL[0..3]) for the block read/verify circuit.

Block Read/Verify. The block read/verify circuit determines the current block type and verify code of the block being read from the tape. This circuit receives the current detect state (DSTATE[3..7]) from the detect state machine, the data verify signals (DVER[0..1]) from the read formatter, and the block type (BT[0..2]) and verify level (VL[0..3]) from the verify count circuit. The current block type (CBT[0..3]) and verify code (VER[0..1]) are sent to the command and status circuit.

Detect State Machine. The detect state machine oversees the reading of blocks from the tape. When given a read command, the detect state machine waits for the start of a block, performs block type detection, waits for the end of the block, then checks the inter-block gap. The detect state machine receives the sync OK signal (SOK), the data record end signal (DREND), the tape mark detect signal (TMDET), the block/gap length signals (BGLEN[0..2]), and the command signals (CMD[0..3]). The detect state machine generates the detect state (DSTATE[0..7]) and the detect flags: short front gap (SFG), noise before detect (NBD), short back gap (SBG), and block overrun (BOVR).

Command/Status. The command/status circuit interfaces the Block Detect circuitry with the Drive Controller. It receives setups and commands and returns status and flags.

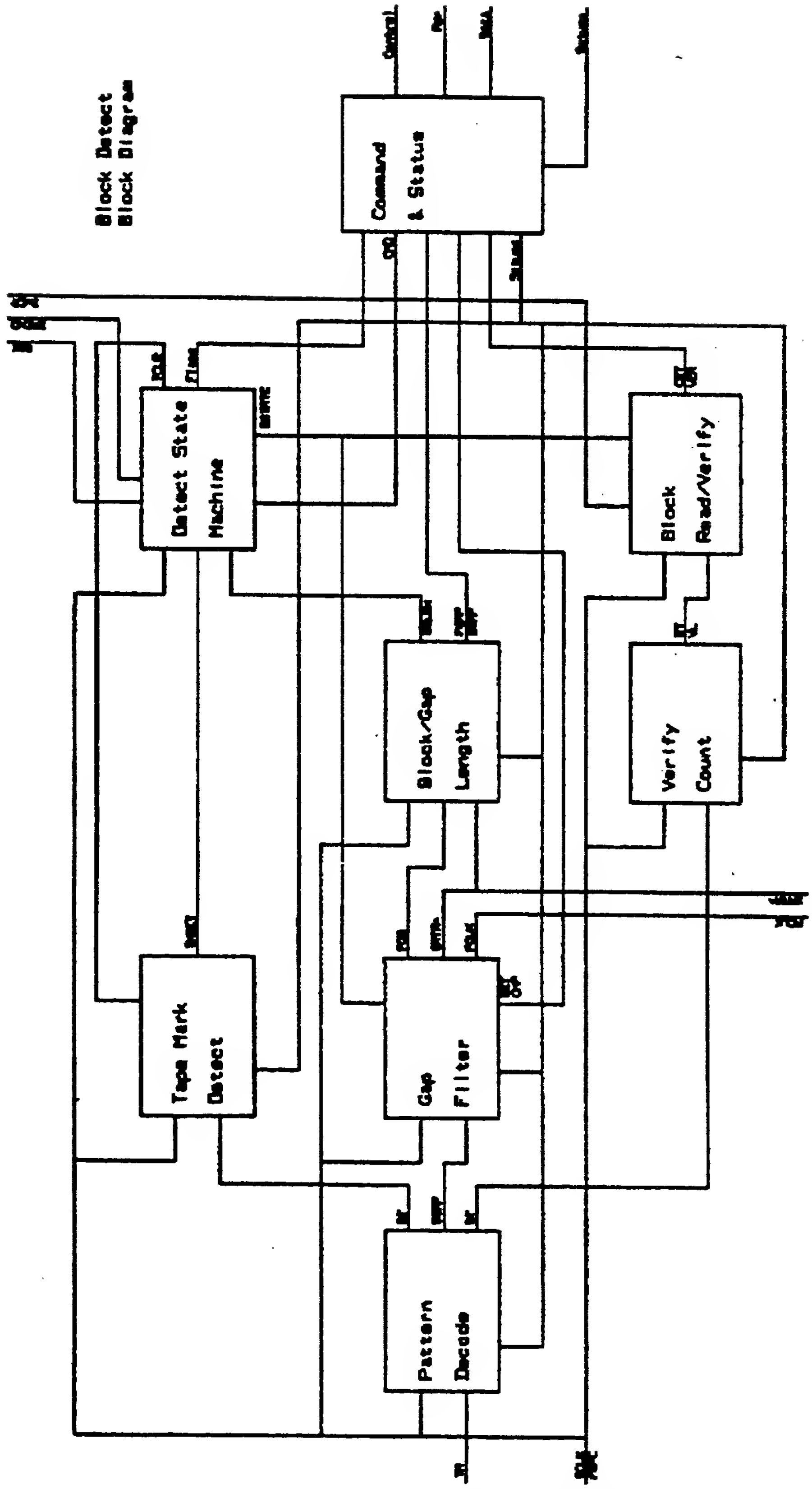

Figure 5-11. Block Detect Block Diagram

5.7 Read/Write PCA

In older units, this PCA was a Read/Write/PLL PCA. The Read Formatter function was on the Formatter PCA (07980-6xx02) in slot #4. After serial number prefix 2805A in the 7979A and 2806A in the 7980A, the read formatting function was placed on the Read/Write/PLL PCA (formerly 07980-6xx01) and only three PCAs were left in the cardcage. The new PCA (in slot #1) then became a Read/Write/Formatter/PLL PCA and the number of the PCA changed to 07980-6xx21 and later to 88780-6xx21. If the drive is configured to use 800 NRZI, this PCA is a 07980-6xx31.

Write Formatter

The Write Formatter on the Read/Write/Formatter/PLL PCA encodes user data from the host computer into flux data to be written on the tape.

The operation of the Write Formatter is managed by software running on the Drive Controller. The Drive Controller initiates the writing of each block on the tape by setting up the Write Electronics then sending a write command to the Write Formatter. The Drive Controller reads the Write Formatter Status following the write of each data record.

The Write Formatter is capable of writing both 1600 cpi Phase Encoded and 6250 cpi Group-Coded Recording ANSI formats. Within these formats data records, tape marks, and ID bursts are written on the tape.

The Write Formatter receives user data from the Data Buffer. The data is encoded into flux data and control marks are added. The flux data is then sent to the Write Electronics to be written on the tape.

The Write Formatter contains seven blocks. These blocks are the Command/Status, the Write Clock Generator, the Test Data Generator, the Data FIFO, the Write Controller, the Write Chip, and the Kill Track. Each block is described by its function, inputs, process, and outputs. The BUCKHORN Write Formatter LSI chip set is used.

Figure 5-12 shows a block diagram of the Write Formatter.

Command/Status

Function: Receive Write Formatter commands from the Drive Controller. Send Write Formatter status to the Drive Controller.

Process: Accept and latch Write Formatter commands from the Drive Controller. Handshake commands to the Write Formatter Controller using command available and data acknowledge. Obtain and the latch parity error and buffer underrun status signals from the Write Formatter Controller. Return this status to the Drive Controller.

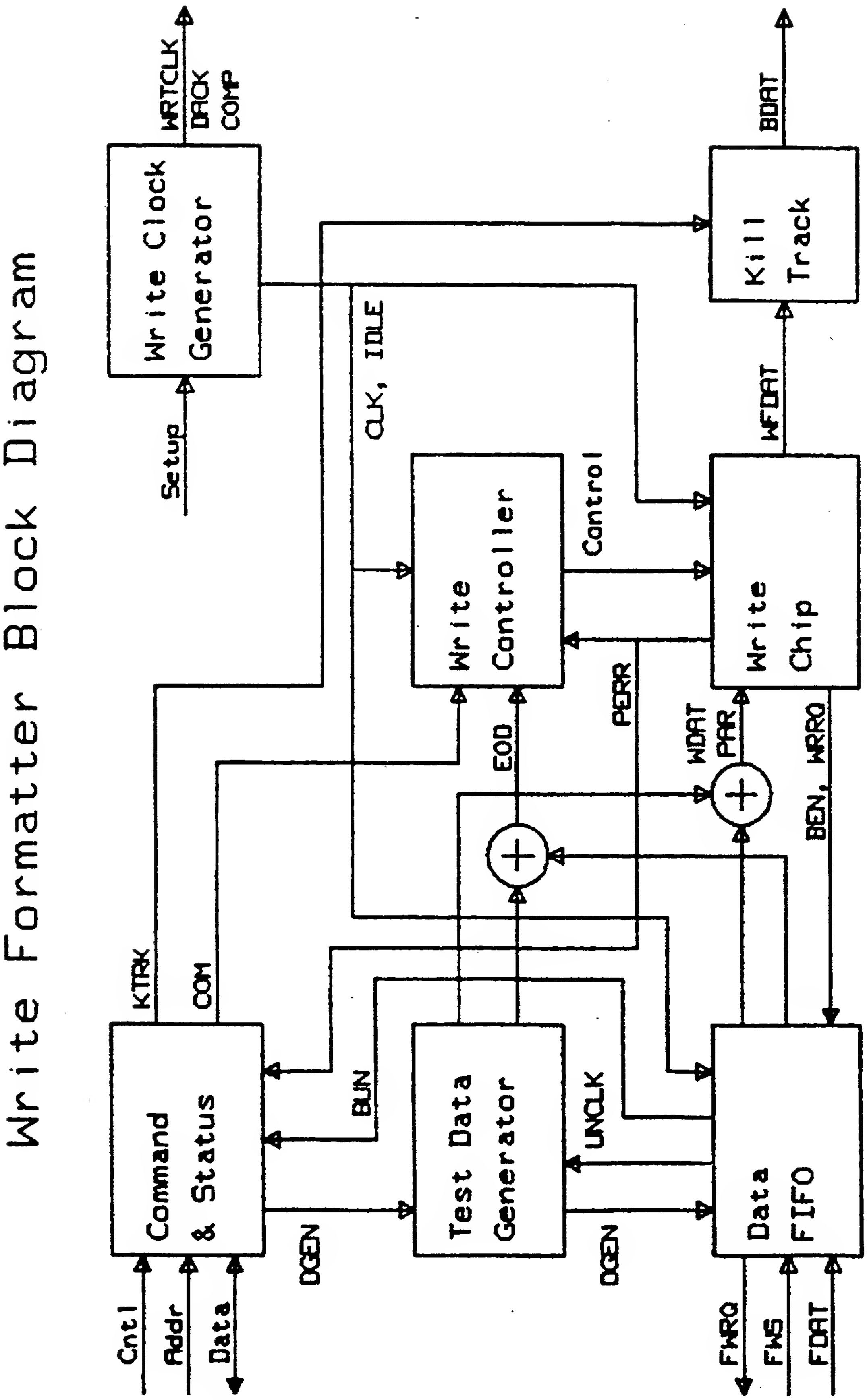

Figure 5-12. Write Formatter Subsystem Block Diagram

Write Clock Generator

Function: Generate clocks for write formatter and write electronics at desired frequency for data format to be written.

Process: Divide down 6.67 MHz clock to provide appropriate clock signals for Write Electronics and Write Formatter. The Write Electronics require a write clock, data clock, and compensate signal at the bit rate required to write on the tape. The Write Formatter requires a 1.67 MHz clock along with the idle and no-op signals to indicate active Formatter clock cycles.

Data FIFO

Function: Receive write data from the Data Buffer then pass it to the write chip.

Process: Send request for a data transfer by holding formatter write request active if there is room in the FIFO. Accept data from the Data Buffer when the formatter write strobe is pulsed true. Hold data in the FIFO until needed by the write chip. Send data to the write chip synchronized to the write formatter clock, idle, and write data request. Send end of data flag with last byte of data.

Test Data Generator

Function: Generate test data for use by the write chip in the writing of data records for diagnostic purposes.

Process: Generate binary data pattern 0 through 255 with odd parity. Send these 256 bytes for each count specified by pattern length. Flag last byte with end of data.

Write Controller

Function: Control the data path contained within the Write Chip.

Process: Receive write commands from Command/Status. These commands include set density, write ID, write tape mark, and write data. Generate the necessary control signals to the Write Chip for execution of each command. These signals include enables for ECC, ACRC, and CRC calculation, clears, mux controls, 4 to 5 conversion controls, and mark generation controls.

Write Chip

Function: Encode data and control marks into flux data for writing either the PE or the GCR format.

Process: For each data block accept data and check its parity. Calculate ACRC, CRC, ECCs, and data groups if writing GCR. Format data block by adding appropriate control marks. For each non data blocks generate the appropriate ANSI standard pattern.

Kill Track

Function: Interface the Write Chip's data path to the Write Electronics.

Process: Accept flux data from the Write Chip. Send data to the Write Electronics. For diagnostics, disable any requested combination of tracks.

Command/Status

The Command/Status block interfaces the Write Formatter with the Drive Controller. This block contains three write registers and one read register. These registers are as follows:

104 Write -	Write Formatter Command Register
105 Write -	Kill Track Control Register
106 Write -	Data Generator Block Size Register
104 Read -	Transfer Status Register

Write Drivers

The write circuits convert digital data into positive and negative write currents.

Each of the nine data signals from the write formatter are turned into two write currents which drive each half of the write coil. The positive half of the write current is generated by signals GCR, PE, and COMP and the negative half by signals GCR*, PE*, and COMP*

These six signals are generated by a PROM for each channel which are driven by common address signals COMP, BP/G*, and DACK. The other two channel-dependent address lines are DATA-1 and DATA-2. DATA-2 lags DATA-1 by a one-bit window time period which allows the PROM to know if the preceeding bit was a zero or a one.

For a data bit equal to one, the GCR signal is on 100% of the bit window time. The PE signal is on 100% of the bit window time if in PE mode and 16% of the bit window if in GCR mode. If the preceeding bit was a zero, the COMP signal is on 80% of the bit window time for GCR mode and 90% of the bit window time for PE mode.

For a data bit equal to zero, the GCR* signal is on 100% of the bit window time. The PE* signal is on 100% of the bit window time if PE mode and 16% of the bit window time if GCR mode. If the preceeding bit was a one, the COMP* is on 80% of the bit window time for GCR mode and 90% of the bit window time for PE mode.

Each of the nine write coil center taps are connected to plus five volts. The other two ends of the coil are each connected to three open collector drivers.

Each open collector is connected to the coil through a current-determining resistor and each open collector driver is controlled by GCR, PE, COMP, GCR*, PE*, or COMP*. Each half-coil current is the sum of three currents generated by pulling the resistors to ground with the open collector drivers.

Erase Drivers

The erase current ramps to steady-state current of 60 mA in less than 0.2 ms and stays at this value until turned off. The erase current is controlled by two circuits which are enabled by WREN, ERASE, and BRNG. One circuit controls the steady-state current and the other circuit is enabled only during the first 0.14 ms that the steady-state circuit is turned on to ensure that the current will be within spec in less than 0.2 ms.

Write/Erase Protection

The protection circuits ensure that the write and erase currents turn on only when commanded to.

The POWER GOOD signal is hard-wired to the input of the protection circuit through a resistor. This signal will not be high until voltages are up to specification and circuits will not turn on until this signal goes high. The write ring signal is buffered and logically ANDed with the buffered write enable signal and the output is connected to the input of the protection circuit. The protection circuit turns on an enhancement mode N-channel MOSFET which is in series with the nine write coil center taps. The same type of circuit is used in the erase circuit to turn on a NPN transistor which provides a ground for the erase circuit.

Read Channel

Circuits in the read channel convert read coil output voltage to digital data.

The read channel consists of seven components; a differentiating pre-amplifier, a gain-controlled amplifier, an automatic gain-control circuit, a zero-cross detector circuit, a zero-cross qualifier circuit, an automatic calibration circuit, and a forth-order Bessel filter.

The input to each channel is the output of a read coil and the output of the read channel is a positive pulse each time the data passes through zero and a

pulse which is logic zero if the data is more negiative than minus 0.10 volts and is logic one if the data is more positive than 0.10 volts. This information is used by the PLL to recreate the digital data as it was recorded.

Differentiating Pre-Amplifier

The pre-amplifier is a 592 differential video amplifier configured as a differentiator. The 200 KHz gain is set for 32 db with a phase shift of 88 degrees and the 555 KHz gain is set for 40 db with a phase shift of 86 degrees. The expected head output of 1 mv P-P to 6.6 mv P-P at 555 KHz results in a final analog output 0.1 V P-P to 0.66 V P-P and the 5 mv PP to 14 mv PP head output at 200 KHz results in a final analog output of 0.175 V P-P to 0.490 V P-P.

AGC Amplifier and AGC Control

The AGC-AMPLIFIER, AGC-CONTROL, ZERO-CROSS DETECTOR, AND ZERO-CROSS QUALIFIER are provided by the National DP8464B disk pulse detector chip.

The pre-amplifier is AC coupled to the AGC-Amplifier which drives the forth-order Bessel filter. The output of the Bessel filter drives the AGC-Control, Zero-Cross Detector, and Zero-Cross Qualifier. The AGC-Control circuit measures the input signal and compares it against an external DC voltage. The difference between these two voltages controls the gain of the AGC-Amplifier to make the peak-to-peak differential voltage output of the Bessel filter equal to four times the external DC voltage.

Zero-Cross Qualifier Circuit

The differentiating pre-amplifier turns peaks into zero-cross data so a comparator can be used to determine when the data peaks. If the signal exhibits a tendency to return to the baseline between peaks the comparator can respond to noise near the baseline. To avoid this problem a Zero-Cross Qualifier circuit is used. This circuit is a comparator with externally-controlled hysteresis. The differential signal must go above or below the DC value before the comparator will switch states. The comparator output is fed to the PLL as zero-cross quailified data.

Zero-Cross Detector Circuit

The output of a bi-directional one-shot is fed to the PLL as zero-cross data which indicates the start of a data window. The PLL uses the zero-cross data to generate a pulse which is 1/2 a bit window long. This pulse is used to clock the zero-cross-qualified data into a latch. The output of this latch represents the sense of the data as it was put on tape.

Bessel Filter

The Bessel filter is a differential input forth-order passive filter which is 1 db down at 587 KHz.

Phase-Lock Loop (Clock Recovery)

The function of the Greeley Clock Recovery Standard Cell Chip (GCRC/1TP2-0001) is to reconstruct the data clock from the data as it is read from tape and converted to digital waveforms by the read electronics. This reconstructed clock is then used by the Formatter to clock the data through the Formatter to the Data Buffer.

Each GCRC chip contains three channels of PLLs with data recognition capabilities. Each channel can handle a bit rate of up to 1.2 Mbits/s. Three chips are used to provide 9-channel capability.

The PLL for each channel is made up of the phase detector, filter, and voltage-controlled oscillator (VCO). Each loop feeds back the DCLK signal to the phase detector where it is compared with the incoming data and correction is applied to the VCO. The amount of correction is determined by the phase detector. The filter integrates the correction signal and filters out high frequency phenomena such as bit-shift, asymmetry, and noise. The resulting error voltage is filtered and applied to the VCO.

The pattern detector is a state machine that recognizes incoming read data and creates control signals based on the pattern. The lock detect (LD) signal is created by the pattern detector and sent to the Formatter. This signal indicates that the PLL has probably locked on to data. Whenever nine "1"s are seen in a row, indicating that a syncronization field has been encountered, the pattern detector sets the LD signal TRUE. A dropout, indicated by nine data windows without data, forces the LD signal FALSE to warn the Formatter that the PLL is about to unlock.

AGC is another signal created by the pattern detector inside the GCRC. This signal is used to select between actual data entering the PLL or the read clock. The "read clock" is the clock created by the GCRC chip. The PLL is forced to lock to this frequency when AGC is a TTL "1". The capability to switch between the two is used to force the PLL to maintain lock to a frequency that is very close to actual data frequency. If the AGC signal is TRUE forcing the PLL to lock to the read clock and data is encountered, the pattern detector sets the AGC signal LOW to allow the PLL to aquire real data. Whenever an extensive dropout occurs (25/PE 41/GCR bits without data), the pattern detector sets AGC forcing aquisition to the read clock.

Another signal created by the pattern detector is the PLOCK signal, which also comes from inside the chip. This signal switches the phase detector between frequency lock and phase lock. When PLOCK is LOW the phase detector outputs error signals proportional to the frequency difference of the DCLK and reference clock. This eliminates the need for padding capacitors and prevents locking on to harmonics of the reference signal. When PLOCK goes HIGH, the phase detector ouputs error signals proportional to the phase difference of the DCLK signal to the reference signal. PLOCK is set TRUE when LD is set TRUE and PLOCK is set FALSE when AGC is set TRUE.

The loop parameters were chosen to optimize performance over the whole spectrum of ANSI specifications for PE and GCR tape formats. The PLL has over 100 percent margin when measured against ANSI specifications.

Automatic Calibration (Autogains)

After each tape is loaded, an autogain is performed when the tape density is being identified or when the tape density ID is being written.

For GCR, the autogain involves all nine tracks during the ARA burst portion of the GCR density ID. For PE, the autogain involves only the PE density identification track.

The autogain sequence is:

1) A reference DAC is stepped from a high gain level to a low gain level while each channel is monitored for the point in which the channel crosses the optimal gain level.

2) This procedure is repeated 2 more times. The data is then sorted for each channel. The median gain for each channel is saved as the "raw gain levels" for the current tape.

3) The average gain of the "raw gain levels" is calculated and saved as the "average gain level" for the current tape.

4) The gain profile for the specific density is loaded from non-volatile RAM and normalized such that its average value across all nine tracks matches the average gain level from the autogain. These gains are referred to as the "current gain levels"

A manual gain profile calibration may be made using Diagnostic Test 99, Read Channel Gain Profile Calibration. Calibration must be performed separately for each density.

5.8 Diagnostics

The diagnostics of the drive are designed to:

Provide predictive information which can lead to early detection of a drive problem.

Provide exhaustive fault isolation tests.

Predictive Diagnostics

Predictive diagnostics make extensive use of runtime logs and runtime error monitoring. All of the key logs are maintained within the non-volatile ram area of the data buffer board. The logs are thereby maintained in spite of power cycling of the drive. The main functions provided with predictive diagnostics are as follows:

Error Log	The drive maintains a history of the past 30 errors that have occurred within the drive, together with a time stamp of when they occurred. The error message maintained for each error indicates the failure and the possible FRUs that may have caused the failure.
Error Rate Log	An error rate log is maintained that contains the number of soft and hard errors, and the number of bytes passed for the past 20 times that a tape was loaded.
Error Rate Warning	During runtime, the most recent entry in the error rate log is monitored. If the error rate becomes too large, an error rate warning will be issued at the front panel. The error rate problem is typically corrected by cleaning the head, but can be an indicator or potential problems.
Cumulative Error Rate	Cumulative number of hard errors, soft errors, and byte count is maintained. This gives service a view of the long past history of the drive error rate.
Tape Odometer	The amount of tape that passed over the head is maintained within an odometer. The odometer aids in monitoring head wear and service pricing.

The logs and monitor variables are all accessible from either the front panel through the use of information and configuration utilities, or remotely through a memory dump and decoding.

Fault Isolation

Isolation of failures within the drive make use of the extensive set of diagnostic tests. The tests are organized as many individual tests which are called and run as sequences of tests. The sequences are ordered to provide the drive with the maximum capability of isolating failures to a single FRU.

With the exception of the Poweron sequence test, the running of tests are not automatic, but require operator intervention to initiate the test. Main test sequences do however provide automatic branching to additional tests to more thoroughly check out a subsystem in which a problem has been detected.

All diagnostic tests within the drive may be initiated from the front panel. With the exception of interactive tests, they may all be exercised remotely also. When a failure is detected, an error message and isolation information is generated, logged and returned to the test initiator whether it be the front panel or remote. A number of additional functions which do not fit directly into predictive and fault isolation diagnostics are provided within the drive.

Combined with diagnostic tests are a number of drive exercisers. The exercisers do not detect or isolate drive failures but are very useful in the diagnostic process by allowing the drive to perform many functions offline or unattended.

The drive is configurable in a number of areas. The set of utilities which display log information and which set up specific diagnostic functions also are used to set up drive configuration.

The drive is designed to support numerous interfaces. With the exception of specific interface tests, all of the diagnostic functions are available on all interfaces.

General Test Descriptions

The three classes of diagnostic tests are the following.

INTERACTIVE CHECKS -	These require operator intervention, and give immediate front panel response indicating the results of the intervention. Checks continue to operate until the reset button is pressed, and always return a diagnostic result of passed. The loop count parameter is ignored during these tests.
EXERCISERS -	These tests cause the drive to perform a specific function to be observed or monitored by the operator. They do not return an error unless an invalid setup prevents the test from operating.
TESTS -	These tests are written such that the drive can detect a failure. A PASS or FAIL is returned on test completion.

Sequences may combine both exercisers and tests, but will typically not include interactive checks because of their need for operator intervention.

A full description of all checks, excercisers, and tests are in Chapter 8, Troubleshooting.

Contents

6

Removal and Replacement

Note

To minimize repetition of procedures, the following removal and replacement instructions are presented as follows:

Instructions are divided into the four general areas where components may have to be accessed;

- The tape deck area (top of the casting)
- The Front Panel area
- Inside the chassis (bottom of the drive)
- The rear panel area.

Common disassembly instructions are given at the beginning of each of these sections and, depending on the component in question, disassembly instructions for specific items continue under a subheading of (A) ... (F). Reassembly instructions for each component are given immediately after the disassembly instructions for that particular component and are in italic type.

Start at the top level of the area that contains the component to be replaced, do the common procedures, and then skip to the specific component desired.

Caution

Use anti-static mats and wrist straps to prevent static damage during repair.

6.1 Tape Deck Area

(A) Printed Circuit Assemblies

Printed Circuit Assemblies

A1. (If the Data Buffer PCA or the battery on the Data Buffer PCA is going to be replaced)

IF POSSIBLE, run Test 128, "Dump Non-Volatile RAM to Tape" before removing power. If Test 128 is not run, all configs will have to be manually reloaded.

A2. Disconnect power from the drive.

A3. Pull the drive out of its rack until the slide rails stop. (Some drives are not in racks.)

A4. Remove the PCA cover on the right side of the casting. Each end of the cover is held by a captive, spring-loaded screw.

Use a flatblade screwdriver to loosen the screws, if necessary.

A5. Remove the PCA(s) as needed. Disconnect the Read and Write Cables from the Read/Write/PLL PCA before removing the PCA. The PCAs are keyed, which assures proper installation.

The 4 PCA version is for 7979As prior to serial number prefix 2805A and for 7980As prior to serial number prefix 2806A.

The 3 PCA version is for 7979As after serial number prefix 2805A and for 7980As after serial number prefix 2806A.

4 PCAs		3 PCAs	
Nearest buffer arm to outer edge of chassis			
Slot 1	Read/Write/PLL	Slot 1	Read/Write/Formatter PLL
Slot 2	Drive Controller	Slot 2	Drive Controller
Slot 3	Data Buffer	Slot 3	Data Buffer
Slot 4	Read Formatter	Slot 4	Empty

Non-Volatile RAM Backup Battery

A6. (If the battery on the Data Buffer PCA is being replaced) remove the battery from the receptacle.

Note

Early data buffer PCAs were shipped with replaceable batteries. After August 1990, Data Buffer PCAs were shipped with non-replaceable batteries. Battery replacement instructions apply to earlier PCAs only.

Warning

The battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire.

Reassembly

A1. (If the battery on the Data Buffer PCA was removed OR if a new Data Buffer PCA is being installed) Check the voltage on the battery. The voltage should be between 2.5 V and 3.0 V. Do not use the battery if the voltage is below 2.5 V.

If the Data Buffer PCA is being replaced, remove the Battery Protect Tab (between the battery and the battery clip). Then test the voltage as explained above.

A2. Re-insert and fully seat the PCA(s).

If the Read/Write/PLL PCA is being inserted, connect the Read and Write Cables to the top edge of the PCA.

A3. Place the PCA cover over the top of the card cage with the captive screws offset toward the tape path. Tighten the screws.

A4. Connect power to the drive. Switch drive ON.

A5. If the Data Buffer PCA was replaced OR if the battery on the Data Buffer PCA was replaced:

1. *Use the customer's configuration tape and run Test 129, "Load Non-Volatile RAM from Tape", to restore any customized*

configurations. **OR** *Load customized configurations from the front panel.*

2. *Use CONFIG 15 to set the battery date in non-volatile RAM.*
3. *Run TEST 99 for both PE and GCR (Parameter A). Make sure Parameter B is on SAVE for both passes of TEST 99. (Use tapes typical of those used at the customer's site.)*
4. *If drive is Option 800 (NRZI), also run TESTs 105 and 106. TEST 105 requires use of a Master Skew Tape (HP p/n 9162-0027) available from DMK.*

A6. *If the Read/Write/PLL PCA is being replaced:*

1. *Run TEST 99 for both PE and GCR (Parameter A). Make sure Parameter B is on SAVE for both passes of TEST 99. (Use tapes typical of those used at the customer's site.)*
2. *If drive is Option 800 (NRZI), also run TESTs 105 and 106. TEST 105 requires use of a Master Skew Tape (HP p/n 9162-0027) available from DMK.*

6.2 Front Panel Area

(A) Front Panel Assembly

(Front Panel Display PCA, Door Interlock Microswitches, Door Solenoid)

A1. Disconnect power.

Caution The Standby Power Switch toggles the transformer 48 volts and may short this line if not disconnected. Ensure that power is removed by disconnecting the power cable.

A2. Pull the drive out of its rack until the slide rails stop. (Some drives are not in racks.)

Front Panel Display PCA

(Does not include removal of PCA)

A3. Raise the top cover.

A4. Remove the screws holding the Front Panel to the chassis.

Two Torx™ screws hold the top of the Front Panel; three hold the bottom of the panel. The panel remains connected to the chassis by many cables at this point.

A5. Remove the cables attached to the front panel.

-Display Control Cable
-Door Solenoid Cable
-Door Sensor Cables
-ON/OFF Switch Cable

Door Interlock Microswitches

A6. Remove the T-9 Torx™ screws that hold the door interlock microswitches.

Door Solenoid

A7. Remove the screw that holds the door solenoid.

Display PCA

A8. Remove two T-9 TORX™ screws.

A9. Remove Display PCA Front Bezel Assembly.

A10. Turn PCA over and remove two T-9 screws from connector shield.

Reassembly

A1. (If the Door Solenoid was removed) Mount the Door Solenoid with the Torx™ screw.

Adjustment:

Adjust the position of the solenoid on its mounting pedestal until there is about 1.5 mm of "play" between the door and the front panel when the door clicks closed.

Grasp each side of the Front Panel and flex the panel a little. The door should not open. Check that the door opens correctly at the end of an UNLOAD sequence.

A2. Install all cables:

-Display Control Cable
-Door Solenoid Cable
-Door Sensor Cable
-ON/OFF Switch Cables

A3. (If the Door Interlock Microswitch was removed) Install the Door Interlock Microswitch.

Caution

Open the top cover before placing the front panel into position. The top door microswitch actuating lever (the plastic extension that projects downward from the right side of the top cover) can break the lever on the front panel door interlock microswitch when the front panel is moved into position.

A4. *(If Display PCA was removed) Install the Display PCA. Be sure to re-attach the connector shield with 2 T-9 screws before installing the display PCA.*

A5. *Position the front panel onto the front of the chassis. Fasten the front panel with the two Torx™ screws on the top and the three on the bottom.*

A6. Lower (close) top cover.

A7. *Connect power.*

A8. *Run the poweron selftest.*

A9. *If the test passes, push the drive back into the unit. If test fails, read error code and refer to Chapter 8 Error Codes for more information.*

6.3 Inside the Chassis

Common steps:

A-to-G 1. Disconnect power.

A-to-G 2. Pull the drive out of its rack until the slide rails stop. (Some drives are not in racks.)

A-to-G 3. Remove the three screws on the lower edge of the front panel.

Note Because of the angle needed to approach these screws, it might be easier to use a T20 screwdriver.

A-to-G 4. Remove the two screws on the bottom cover plate near the front and rotate the bottom plate away from the chassis. (The back edge of the cover plate is inserted into the rear panel frame; the plate has to be pulled forward a little to come free of the frame.)

(A) Motor/Power PCA

A5. Remove the ribbon cable that goes from the Motor/Power PCA to J41 on the Mother PCA (in the card cage). Set this cable aside.

A6. Detach the seven connectors on the Motor/Power PCA.

A7. Remove the six screws the hold the PCA to the casting. Because of the location of these screws, a long (at least six inch) Torx™ screwdriver is needed.

A8. Slide the Motor/Power PCA out from the chassis.

Reassembly

A1. Slide the Motor/Power PCA into place and fasten it to the chassis with the six Torx™ screws.

A2. Attach the seven cable connectors.

A3. Connect the Motor Drive Ribbon Cable to J41 on the Mother PCA.

A4. *Slide the bottom cover plate into the rear panel frame and bring the bottom cover plate into position. The tabs along the sides should enter the slots in the side rails.*

A5. *Fasten the lower edge of the front panel with three Torx™ screws.*

A6. *Connect power.*

A7. *Run Test 2, "Wellness" Test.*

A8. *If the test passes, push the drive back into the rack. If test fails, read error code and refer to Chapter 8 Error Codes for more information.*

(B) Sensor PCA

B5. Remove the screws from two Tape-in-Path Sensors and pull sensors away from casting.

Note

At this point, the Sensor PCA is still attached to the casting by a single screw and to the Front Panel by the Tape Door Open Sensor wires. The connectors for these wires are located next to the tape door; not accessible until the Front Panel is moved away from the chassis.

To change sensor wires without having to completely remove the Front Panel (and have to disconnect all the connectors to the panel), get the new Sensor PCA and refer to the following "Reassembly" instructions.

Reassembly:

B1. *Thread the connectors for the Door Open Microswitch Cable into the Front Panel PCA area and temporarily store them there.*

B2. *Switch the old Door Open Microswitch Cable wires for the new set:*

-Remove the two screws from the top of the Front Panel
-Move the Front Panel far enough away from the chassis to reach in and remove the two Door Open Sensor wires from the bayonet connectors on the Door Open Sensor microswitch

-Retrieve the new Door Open Sensor wires from where you stored them (in the vicinity of the Front Panel PCA) and connect these wires to the Door Open Sensor microswitch - let the new Sensor PCA hang free

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Caution Open the top cover before placing the front panel into position. The top door microswitch actuating lever (the plastic extension that projets downward from the right side of the top cover) can break the lever on the front panel door interlock microswitch when the front panel is moved into position.

-Place the Front Panel back in position, insert and tighten the two screws that hold the top of the Front Panel to the chassis.

B3. *Remove the screw that holds the old Sensor PCA to the casting. Remove the PCA along with two Tape-in-Path-sensor wires and the Tape Door Open Sensor wires.*

B4. *Place the new Sensor PCA into position, insert and tighten the screw that holds it to the casting.*

B5. *Put the two Tape-in-Path Sensors into position, insert and tighten the screw that holds each sensor into place.*

B6. *Slide the bottom cover plate into the rear panel frame and bring the bottom cover plate into position. The tabs along the sides should enter the slots in the side rails.*

B7. *Fasten the lower edge of the front panel with three Torx™ screws.*

B8. *Connect power.*

B9. *Load a tape.*

B10. *If a tape loads correctly, push the drive back into the rack.*

(C) Head Plate Assemblies

(Speed Encoder, Tape Displacement Unit, Buffer Arm Assembly, Heads/frame) Buffer Arm Assembly is: Buffer Arm, BOT/EOT Assembly

Speed Encoder

C5. Remove the Speed Sensor cable assembly at the Mother PCA.

C6. Remove the three Torx™ screws that hold the Speed Encoder baseplate to the casting.

C7. Pull the Speed Sensor and cable up through the casting.

Reassembly:

C1. Put the Speed Sensor and cable through the casting with the tape deflector closest to the tape path guide.

C2. Insert and tighten the three Torx™ screws that hold the Speed Encoder baseplate to the casting.

C3. Attach one end of the Speed Sensor cable to the bottom of the Speed Encoder and the other end to the connector labeled "ENCODER" on the Mother PCA.

C4. Slide the bottom cover plate into the rear panel frame and bring the plate into position. The tabs along the sides should enter the slots in the side panels.

C5. Insert and tighten the two screws on the front-panel end of the bottom cover plate.

C6. Insert and tighten the three screws on the lower edge of the front panel.

Tape Displacement Unit (TDU)

C5. Remove the two wires from the bayonet clips on the Tape Displacement Unit.

Caution DO NOT LOOSEN OR REMOVE THE POZIDRIV™ SCREWS ON THE HEAD PLATE ASSEMBLY. These screws set the head skew adjustment. This is a factory adjustment only.

C6. Remove the two Torx™ screws that hold the Tape Displacement Unit in place and remove the Unit.

Reassembly:

C1. Position the Tape Displacement Unit so that the rod passes between the Head and the Tape Cleaner Block.

C2. Insert and tighten the two Torx™ screws that hold the Tape Displacement Unit in place.

C3. Attach the two wires to the bayonet clips on the Tape Displacement Unit.

Buffer Arm Assembly

(Buffer Arm, BOT/EOT Assembly)

Buffer Arm

C5. Remove the Motor Drive Ribbon Cable from J41 on the Mother PCA and J2 on the Motor/Power PCA.

Note The next two cables have capture clips. Press the release on the connector before attempting to remove it.

C6. Remove the Buffer Arm position sensor cable from the connector marked "TENSION" on the Mother PCA (J61).

C7. Remove the Buffer Arm BOT/EOT sensor cable from the connector marked "BOT/EOT" on the Mother PCA (J51).

C8. Disconnect the spring from the Buffer Arm.

C9. Remove the three screws that hold the Buffer Arm baseplate to the casting.

C10. Pull the Buffer Arm Assembly out of the casting (the BOT/EOT Sensor Assembly remains attached to the Buffer Arm baseplate).

BOT/EOT Sensor Assembly
(BOT/EOT Sensor, Buffer Arm Position Sensor)

Note All steps under "Buffer Arm" removal above must be done (i.e. common steps plus C5 though C10).

C11. Remove the screw that holds the BOT/EOT Sensor Assembly to the Buffer Arm baseplate.

C12. Lift the BOT/EOT Sensor assembly away from on the Buffer Arm Baseplate. You may have to wiggle the assembly a little and also rotate the Buffer Arm a little to loosen the assembly.

Reassembly

Note Whether the BOT/EOT Sensor is replaced or the Buffer Arm is replaced (retaining the good BOT/EOT Sensor), re-assembly remains the same.

C1. Put the BOT/EOT Sensor assembly over the metal flag near the hub of the Buffer Arm.

C2. Position the sensor.

The locator pin on the bottom of the sensor goes in the hole on the Buffer Arm baseplate. Adjust as necessary to align the mounting screw hole on the sensor over the hole on the Buffer Arm baseplate. If everything is aligned, the sensor assembly should fit into the depression machined out of the Buffer Arm baseplate.

C3. Insert screw to hold BOT/EOT Sensor Assembly in place on the Buffer Arm.

C4. Insert the assembly into the casting.

The sensor cable (coming out from the bottom of the arm) goes directly through the hole. The EOT/BOT cable (the wider cable) goes alongside through the gap in the casting.

C5. *Insert and tighten the the three screws that mount the Buffer Arm baseplate to the Head Plate.*

C6. *Put the spring back on the the pin of the Buffer Arm.*

C7. *Attach the Buffer Arm BOT/EOT sensor cable to the connector marked "BOT/EOT" on the Mother PCA (J51).*

C8. *Attach the Buffer Arm position sensor cable to the connector marked "TENSION" on the Mother PCA (J61).*

Caution

Do not install the Motor Drive Ribbon Cable backwards in its connectors. Be sure to put the cable connector keys into the key SLOTS on the Motor/Power PCA and the Mother PCA connectors. The side opposite to the slotted side of these PCA connectors is open and can act as a slot.

C9. *Attach the Motor Drive Ribbon Cable to J41 on the Mother PCA and J2 on the Motor/Power PCA.*

Head Plate Assembly

(Speed Encoder, Buffer Arm/Speed Sensor, Tape Displacement Unit, Cleaner Block, Head w/Plate Assembly)

Removing the Head Plate Assembly

C5. Disconnect and move aside all cables from the visible portion of the Mother PCA that is nearest the rear of the chassis:

Note

Some cables have capture clips. Press the release on the connector before attempting to remove it.

-Motor Drive Ribbon Cable (J41)
-BOT/EOT ribbon cable from the connector marked "BOT/EOT" (J51)
-Buffer Arm Position Sensor ribbon cable from the connector marked "TENSION" (J61)

-Speed Encoder ribbon cable from the connector marked "ENCODER" (J71)
-Interface ribbon cable from J81.

C6. Disconnect the two bayonet connections to the Tape Displacement Unit.

C7. Open the two plastic cable retaining clips that hold the Read and Write Cables to the side of the card cage.

C8. Disconnect the Read Cable and the Write Cable from the top of the Read/Write/PLL PCA.

C9. Remove the Read/Write/PLL PCA from the card cage. (This makes it easier to pull the cable connections back through the card cage.)

C10. Remove the Buffer Arm/BOT/EOT Sensor Assembly.

C11. Remove the three Torx™ screws that hold the Head Plate Assembly to the casting.

Caution Cover the tape head during removal. The head can be easily scratched (a piece of 1 inch wide masking tape works well for this. Remember to remove the masking tape and clean the head completely to remove any adhesive residue).

C11. Pull the Head Plate Assembly out of the chassis, carefully pulling the Read and Write Cables through the card cage on the way out.

Reassembly:

Caution Cover the tape head during reassembly. The head can be easily scratched.

C1. Place the Head Plate Assembly into its position in the casting; thread the Read and Write Cables into the card cage as the Head Plate Assembly is put into position. The Read and Write Cable connectors should face the PCAs in the card cage.

C2. Insert and tighten the three screws that hold the Head Plate Assembly to the casting.

C3. *Insert the Read/Write/PLL PCA into the card cage.*

C4. *Connect the Buffer Arm/Speed Sensor to the Head Plate.*

C5. *Connect the Read Cable and the Write Cable to the Read/Write/PLL PCA.*

C6. *Fasten the two plastic cable retaining clips that hold the Read and Write Cables to the side of the card cage.*

C7. *Connect the two Tape Displacement Unit wires.*

C8. *Connect all of the cables to the Mother PCA:*

Caution Do not install the Motor Drive Ribbon Cable backwards in its connectors. Be sure to put the cable connector keys into the key SLOTS on the Motor/Power PCA and the Mother PCA connectors. The side opposite to the slotted side of these PCA connectors is open and can act as a slot.

-Motor Drive Ribbon Cable to J41
-BOT/EOT ribbon cable to the connector marked "BOT/EOT" (J51)
-Buffer Arm Position Sensor ribbon cable to the connector marked "TENSION" (J61)
-Speed Encoder ribbon cable to the connector marked "ENCODER" (J71)
-Interface (or Slave) ribbon cable to J81 (or J91).

C9. *Slide the bottom cover plate into the rear panel frame and bring the plate into position. The tabs along the sides should enter the slots in the side rails.*

C10. *Insert and tighten the two screws on the front-panel end of the bottom cover plate.*

C11. *Insert and tighten the three screws on the lower edge of the front panel.*

C12. *Connect power.*

C13. *Run Test 2, "Wellness" Test.*

C14. *Run Test 99, "Read Channel Calibration Test" with parameter B on SAVE to retain head gain values in non-volatile RAM.*

C15. If drive is Option 800 (NRZI) run Test 105 and 106. Test 105 requires use of a master skew tape (HP p/n 9162-0027) available from DMK.

C16. If applicable, push back into the cabinet.

(D) Motors and Hubs

Supply Motor and Hub, Takeup Motor and Hub

Note The Supply and Takeup Motors and hubs are removed in the same way.

D5. Disconnect the applicable motor power cable from the Motor/Power PCA. The Supply Motor connector is J1 and the Takeup Motor connector is J3.

D6. Loosen the flathead screw in the center of the hub. The screw does not have to be removed; it can be held by the hub as you take the hub off.

Older models use use a #10-24x0.625 T20 screw in the hub. New units have use a #10-24x0.50 hardened T25 screw.

D7. Lift the hub off.

D8. Loosen the four T25 screws that hold the motor.

D9. Rotate the motor until the screws enter the wide part of the slot in the casting.

Caution When removing the Supply Motor, it is possible to catch the Sensor PCA with one of the motor mounting screws.

D10. From underneath, pull the motor away from the casting.

Reassembly:

D1. Place the motor into position, passing the T25 mounting screws through the large part of the screw slot.

Caution When inserting the Supply Motor, make sure that Sensor PCA is not scraped by one of the mounting screws.

D2. *Rotate the motor until the mounting screws go to the end of the narrow part of the slot.*

D3. *Tighten the mounting screws.*

D4. *Slide the hub onto the motor shaft.*

D5. *Tighten the T25 (or T20 in older units) flathead screw.*

D6. *Connect the applicable motor power cable to the Motor/Power PCA. The Supply Motor cable connects to J1 and the Takeup Motor Cable connects to J3.*

D7. *Slide the bottom cover plate into the rear panel frame and bring the bottom cover plate into position. The tabs along the sides should enter the slots in the side panels.*

D8. *Fasten the lower edge of the front panel with three Torx™ screws.*

D9. *Connect power.*

D10. *Perform Test 2, "Wellness" Test.* If test fails, read error code and refer to Chapter 8 Error Codes for more information.

D11. *If the test passes, push the drive back into the rack.*

(E) Blower Motor

E5. Disconnect the Motor Drive Cable from the Motor/Power PCA (J2).

E6. Disconnect the Takeup Motor Power Cable from J3 on Motor/Power PCA.

E7. Disconnect the connector from J5 on the Motor/Power PCA.

E8. Disconnect the Mother Board PCA Cable from J4 on Motor/Power PCA.

E9. Disconnect the connector on the fan power leads. You may have to cut a plastic wire wrap to release the power leads from the bundle.

E10. Release the six plastic clips that hold the fan to the plenum starting with the clips near the center of the drive chassis.

E11. Remove the blower fan FRU from the chassis.

Reassembly:

E1. Set the Blower Fan FRU into the plastic clips near the outside of the chassis. Push the top of the blower fan into the clips that hold the assembly. Make sure the clips snap into place

E2. Connect the blower fan power connector.

E3. Connect the long connector to J5 on the Motor/Power PCA.

E4. Connect the Motor Drive Cable to the Motor/Power PCA (J2).

E5. Connect the Takeup Motor Power Cable to the Motor/Power PCA (J3)

E6. Connect the Mother Board Connector to the Motor/Power PCA (J4)

E7. Slide the bottom cover plate into the rear panel frame and bring the bottom cover plate into position. The tabs along the sides should enter the slots in the side rails.

E8. Fasten the lower edge of the front panel with three Torx™ screws.

E9. Connect power.

E10. Load a tape to test the blower motor.

E11. Push the drive back into the unit.

(F) Hub Lock Assembly

(Hub Lock Actuator Lever, Solenoid)

Hub Lock Actuator Lever

F5. Remove Front Panel (See Steps A3 through A5 oc section 6.2).

F6 Remove the two solenoid power cables. These power cables may be disconnected at a clip connection near the Supply Motor on older units.

F7. Remove the screw that holds the solenoid to the casting.

F8. Remove the screw at the Hub Lock Arm pivot point.

Reassembly:

F1. *Position the Hub Lock Arm and insert the screw into the pivot point. Tighten the screw.*

F2. *Insert and tighten the screw that holds the solenoid to the casting.*

F3. *Connect the two solenoid power cables at the clip connection near the Supply Motor.*

F4. *Slide the bottom cover plate into the rear panel frame and bring the bottom cover plate into position. The tabs along the sides should enter the slots in the side rails.*

F5. *Install the Front Panel Assembly.*

F6. *Connect power.*

F7. *Load a tape to test the lock solenoid.*

F8. *If the hub locks properly, push the drive back into the unit.*

6.4 Rear Panel Area

(A) Interface PCA (all interfaces)

A1. Disconnect power.

Caution Use anti-static mats and wrist straps to prevent static damage during repair.

A2. Remove the two interface panel mounting screws.

A3. Rotate the panel far enough out to gain access to the power and ribbon cables.

A4. Disconnect the power cable and the ribbon cable.

A5. Rotate the Interface PCA clear of the rear panel. (Two tabs at the bottom of the PCA panel fit into two slots on the lower edge of the chassis.)

Reassembly:

A1. Put the tabs on the Interface PCA panel into the slots in the chassis. Rotate the PCA panel close enough to the chassis to allow connection of the power cable and ribbon cable. Connect the cables.

A2. Connect the two cables.

A3. Insert and tighten the two screws that hold the Interface Panel onto the rear of the unit.

A4. Connect power.

A5. Run the Test 12, Interface Specific Test.

A6. If the test passes, push the drive back into the unit. If test fails, read error code and refer to Chapter 8; Error Codes for more information.

(B) Fuses (in the rear panel fuse receptacle)

B1. Insert the tip of a small screwdriver (or similar tool) into the small slot on the edge of the fuse receptacle and dislodge the fuse module. Pull the module out.

Reassembly:

Caution Replace the fuse with one of an identical rating.

Caution In the next step, make sure that the white arrow on the fuse module lines up with the desired voltage rating printed on the fuse module receptacle.

B1. Slide the fuse module into its receptacle.

(C) Cooling Fan

C1. Disconnect power.

C2. Pull the drive out on its rack.

C3. Remove the center screw on the lower edge of the front panel.

Note Because of the angle needed to approach this screw, it might be easier to use a T20 screwdriver.

C4. Remove the two screws on the bottom cover plate near the front and rotate the bottom plate away from the chassis. (The back edge of the cover plate is inserted into the rear panel frame; the plate has to be pulled forward a little to come free of the frame.)

C5. Follow the red and black power wires from the side of the cooling fan along the large bundle of wire-wrapped wires until you reach a snap

connector (connector should be located near the side of the power transformer). Disconnect the snap connector.

C6. Cut enough of the wire wraps on the large bundle of wires to release the red and black fan wires.

C7. Remove the four T25 screws that hold the fan onto the rear panel.

C8. Slide the fan down and out of the chassis. Part of the lower edge of the rear panel frame is cut away enough to allow the fan to slide out.

Reassembly

C1. Slide the fan into position behind the rear panel. The red and black power wires face toward the Interface Assembly. The airflow arrow must point to the rear of the drive (the exhaust exits through the rear panel).

C2. Fasten the fan to the rear panel with four T25 screws.

C3. Connect the fan power connector. Make sure the clip is snapped securely.

C4. Route the fan power wires next to the large wire bundle in front of the fan. Wire-wrap the wires as necessary.

C5. Slide the bottom cover plate into the rear panel frame and bring the bottom cover plate into position. The tabs along the sides should enter the slots in the side rails.

C6. Fasten the lower edge of the front panel with three Torx™ screws.

C7. Connect power.

C8. Turn the drive ON.

C9. Check that the fan is operating properly.

C10. Run Test 2, "Wellness" Test.

C11. If the test passes, push the drive back into the rack. If test fails, read error code and refer to Chapter 8; Error Codes for more information.

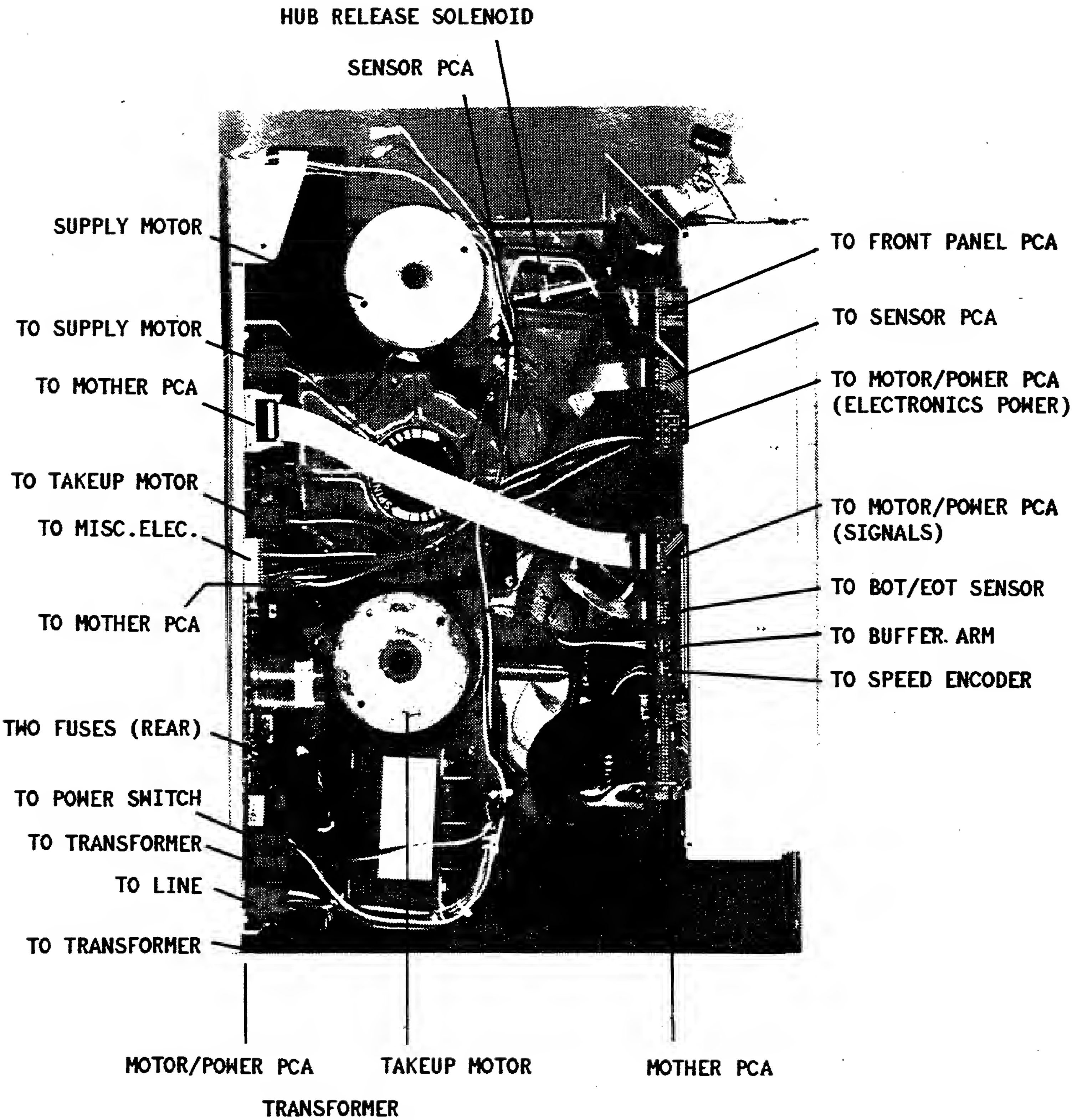


Figure 6-1. Inside the Chassis

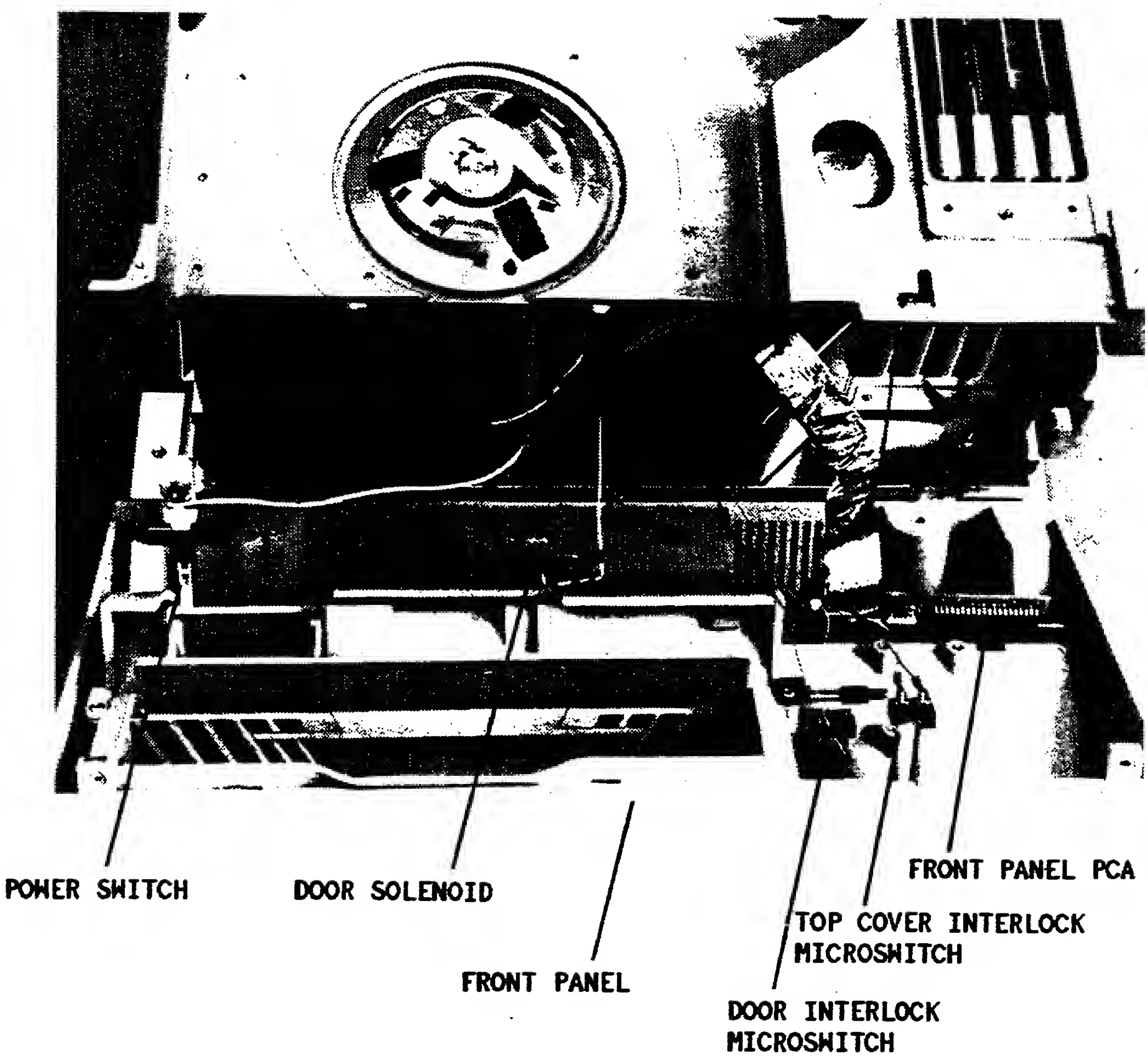


Figure 6-2. Inside the Front Panel

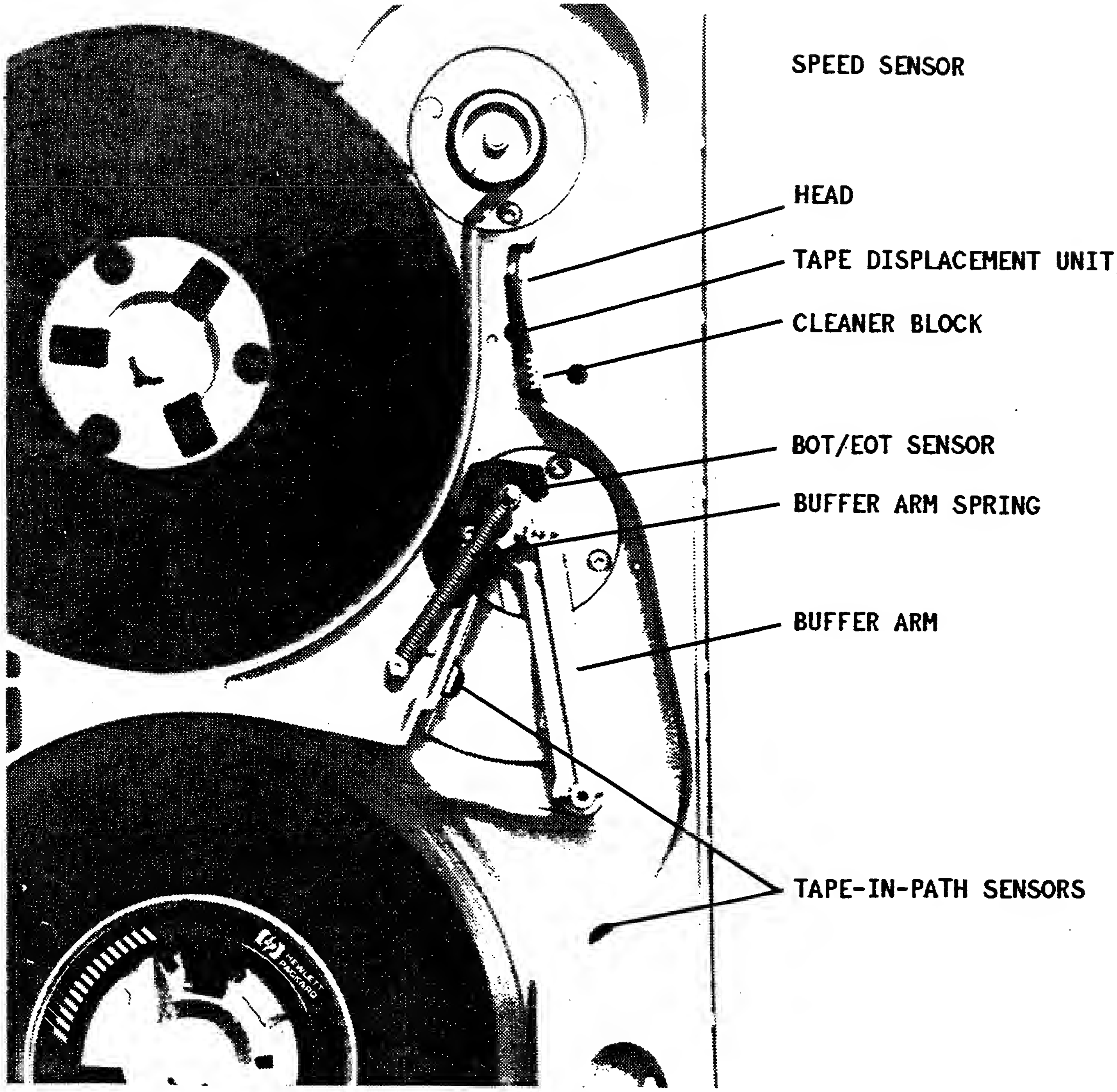


Figure 6-3. Tape Path Components

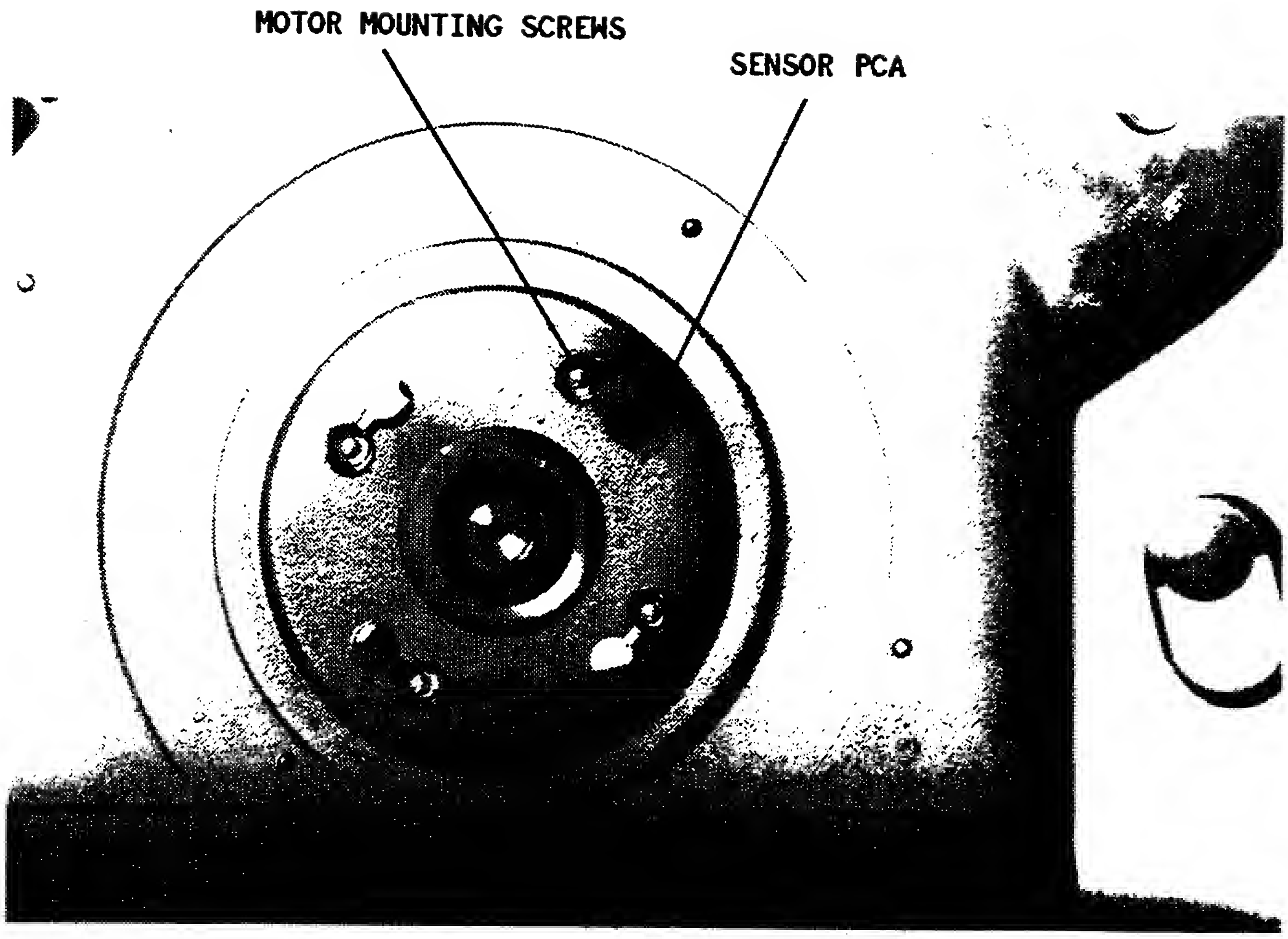


Figure 6-4. Supply Motor Mounting and Sensor PCA

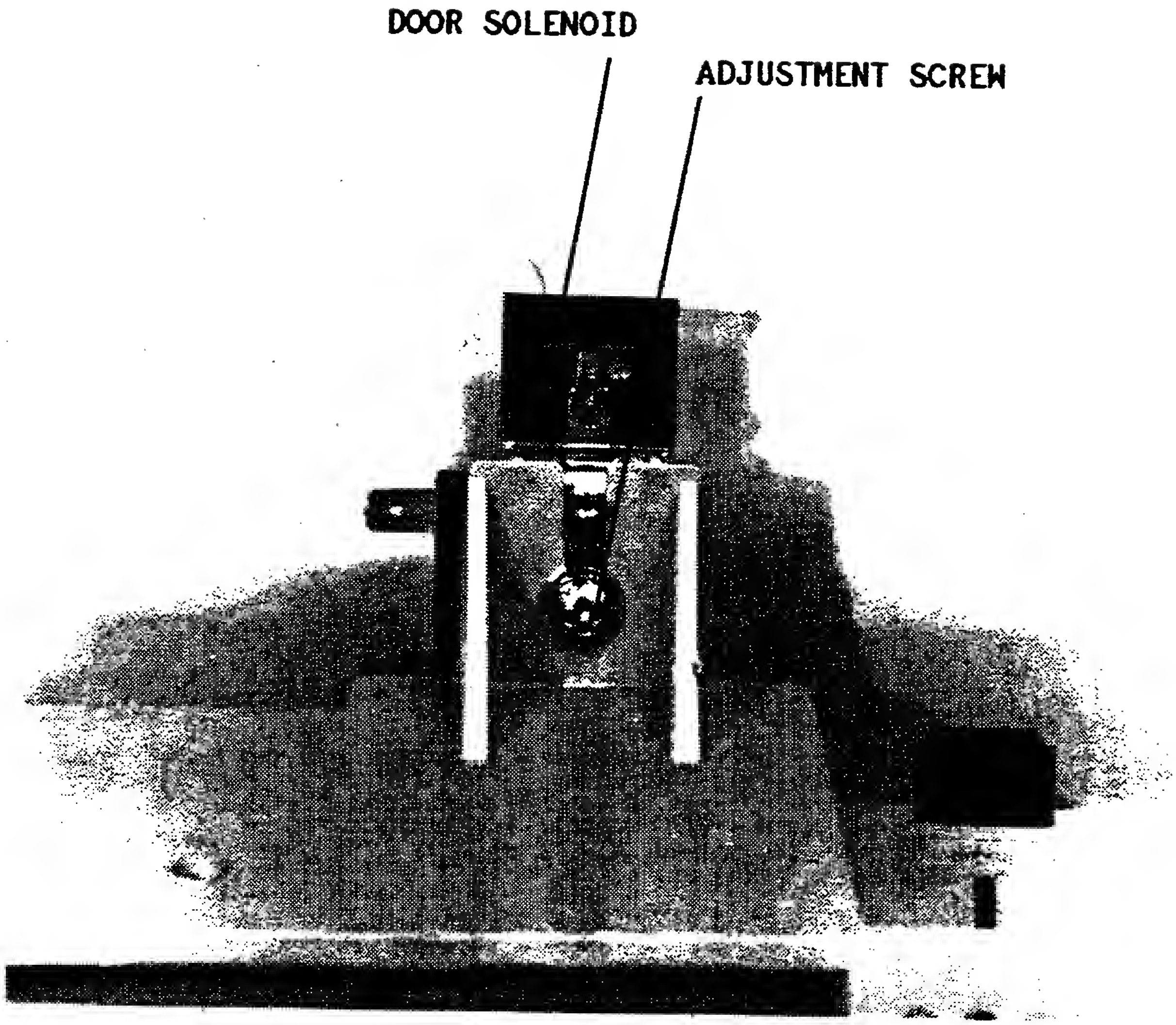


Figure 6-5. Tape Door Solenoid Adjustment Screw

7

Adjustments

7.1 Installing Firmware Kits

Materials Required

-Electrostatic Discharge (ESD) groundstrap
-ESD mat
-Torx™ T25 screwdriver
-#2 Pozidriv™ screwdriver
-(if HP-IB interface) 7mm hex driver
-(if SCSI interface) #1 Pozidriv™ screwdriver

Save the Drive Logs and Configurations in Non-volatile RAM

1. Apply power to the drive.
2. Select INFO 0.
3. Write down the drive logs. These are to be kept as part of the drive repair records. There may be up to 30 drive logs.
4. Verify that special customer configurations were logged at installation. These will have to be re-entered from the front panel.
5. "DOWN" the drive from the system console. (For HP Systems only. For other systems, check the host manual.)

Remove Power from the Drive

1. Remove the power cord from the drive.
2. Remove the interface cable from the drive (HP-IB, SCSI, Pertec-compatible).

Caution During the next part of the installation, observe ESD precautions. Do not lay the PCAs on the plastic top cover. This cover is not electrically conductive and may hold a charge.

Replace EPROMS on the Data Buffer PCA

1. Remove the RFI cover.
2. Remove the Data Buffer PCA from the card cage
3. Change the EPROMs.

   For the Data Buffer PCA **07980-69004:**

   a. Remove the two EPROMS from sockets U603 and U803.

   b. Install the EPROM labeled U602-504 in socket U603.

   c. Install EPROM labeled U803-504 in socket U802.

   d. Re-insert the Data Buffer PCA in the card cage.

   For the Data Buffer PCAs **07980-69014, 07980-69024, and 07980- 69034:**

   a. Remove the two EPROMS from sockets U502 and U602.

   b. Install the EPROM labeled U502-5x4 in socket U502.

   c. Install EPROM labeled U602-5x4 in socket U602.

   d. Re-insert the Data Buffer PCA in the card cage.

Replace EPROMS on the Drive Controller PCA

1. Remove the Drive Controller PCA from the card cage.
2. Change the EPROMs.
   a. Remove the three EPROMS from sockets U1, U4, and U19.
   b. Install EPROM labeled U1-503 in socket U1.
   c. Install EPROM labeled U4-503 in socket U4.
   d. Install EPROM labeled U19-503 in socket U19.
   e. Re-insert the Drive Controller PCA into the card cage.

Replace EPROM on the Interface PCA

1. Remove the Interface Assembly from the rear of the drive.
   a. Remove the two Torx™ screws that hold the interface to the rear panel of the drive (either side of the top of the interface).
   b. Rotate the interface plate out and disconnect the two cable connectors (2-pin and 50-pin) from the PCA.
   c. Place the Interface Assembly on the ESD mat.
2. Detach the interface cable connections from the metal panel (HP-IB and SCSI only).
   a. If HP-IB, remove the two 7mm hex nuts from each end of the connector.
   b. If SCSI, use a #1 Pozidriv™ to remove the four screws holding the two connectors. See the next figure.

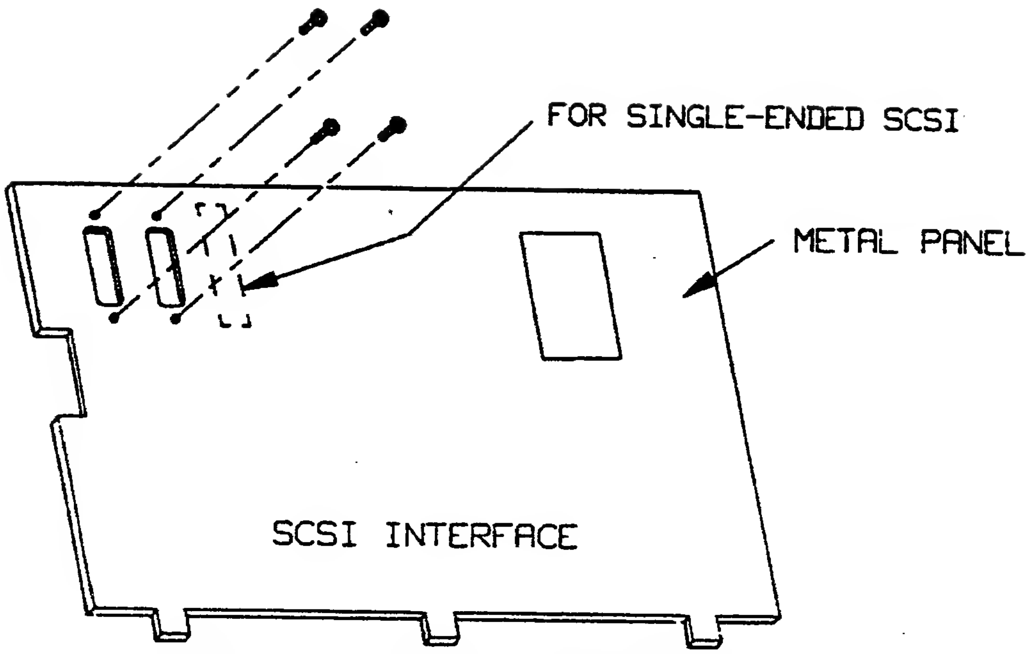


Figure 7-1. Screws on the SCSI Connectors.

3. Remove the interface PCA from the metal panel.

   a. Turn the assembly over (metal panel facing down towards the mat). Use a #2 Posidriv™ screwdriver to remove the five screws (HP-IB, SCSI interface) or 6 screws (Pertec-compatible interface) that hold the printed circuit board to the metal panel.

      If you are working with a SCSI interface, DO NOT REMOVE the four #1 Pozidriv™ screws holding the SCSI connectors to the circuit board.

      Refer to Figure 7-2 for the SCSI and HP-IB interface mounting screws. Refer to Figure 7-3 for the mounting screws on the Pertec-compatible interface.

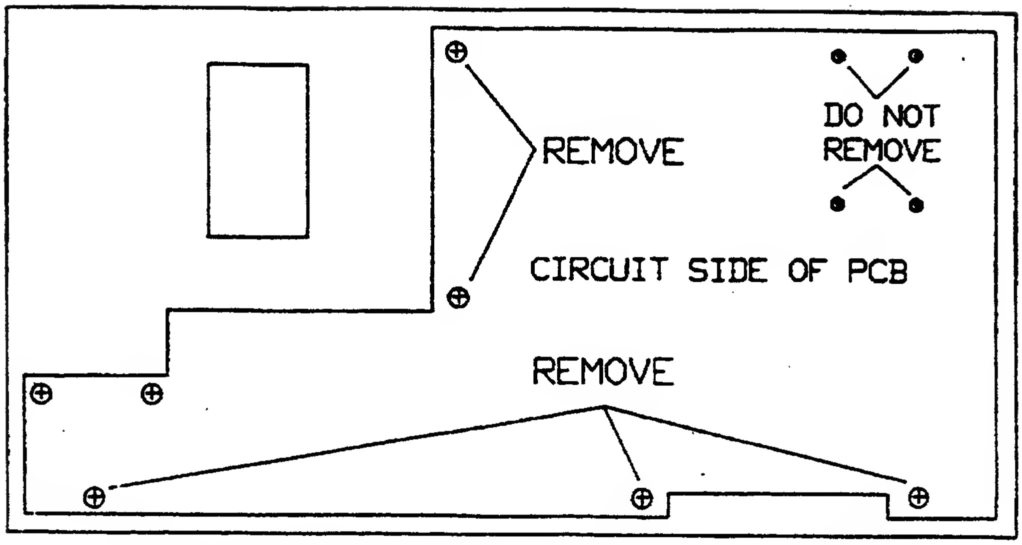


Figure 7-2. SCSI and HP-IB PCA Mounting Screws.

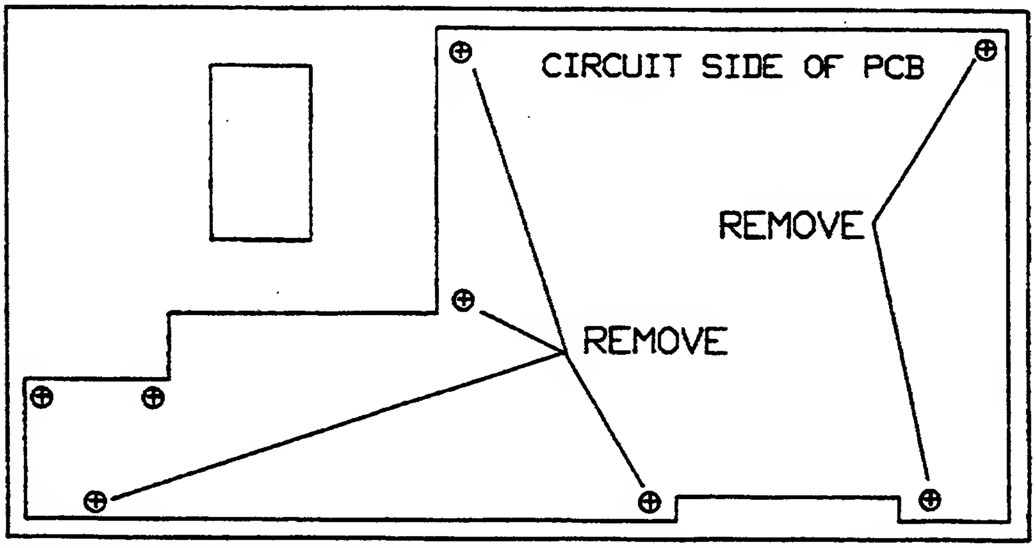


Figure 7-3. Pertec-compatible Interface PCA Mounting Screws.

4. Lift the printed circuit board up off the metal panel. Move the metal panel aside.
5. Turn the printed circuit board over, placing the circuit side on the ESD mat. Place the board on the mat so that the interface connectors are facing away from you. See Figure 7-4.

   When the board is properly oriented, the internal bus cable connector is on the lower right side.

The large integrated circuit on the lower left side is the MC68B09 microprocessor. Just off the upper left corner of the microprocessor is the 28-pin socket U12 that will hold the EPROM.

6. Remove the current EPROM from:

   -socket U12 (on HP-IB) or

   -socket U51 (on SCSI) or

   -socket U13 (on Pertec-compatible).

7. Install the new EPROM

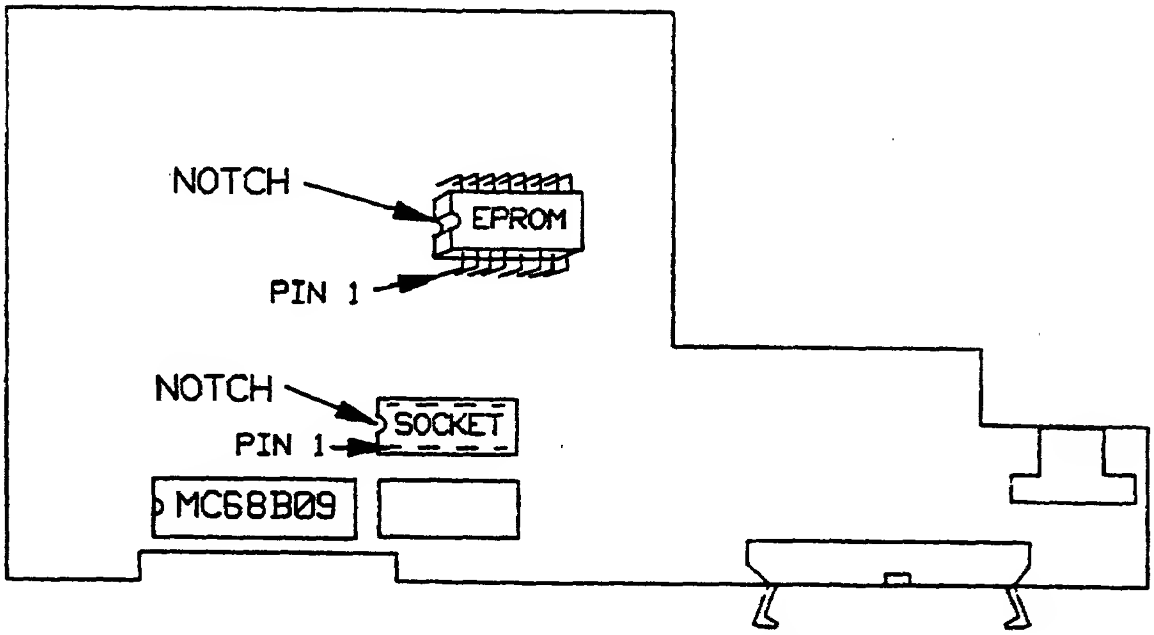


Figure 7-4. EPROM location on all interfaces.

Caution

Insert the EPROM into its socket correctly. The 28-pin socket for the EPROM has a notch on its left side (the end facing the microprocessor). The EPROM also has a notch on one end. Be sure to have these notches line up when inserting the EPROM.

---

8. Install the interface EPROM in the 28-pin socket.

9. **(HP-IB)** If the interface is HP-IB, this would be a good time to verify that the loads are correct for the system. An explanation of HP-IB loading is in Chapter 3.

10. Install the interface assembly metal panel.

    a. Place the metal panel on the component side of the interface board.

    b. Hold the metal panel and interface board together and turn them over. When layed back down on the mat, the circuit side of the board is on top.

    c. Re-attach the interface board to the metal panel using the #2 Pozidriv™ screws removed during disassembly.

11. (HP-IB) Re-install the two 7mm hex nuts that hold the connector to the metal plate.

12. (SCSI) Re-install the four #1 Pozidriv™ screws that hold the SCSI connectors to the metal plate.

13. (Pertec-compatible) Inspect the connectors. The two rows of connectors should line up with the slots at the ends of the connector holes (see Figure 7-5). Apply gentle pressure as necessary to line up the connectors into the slots.

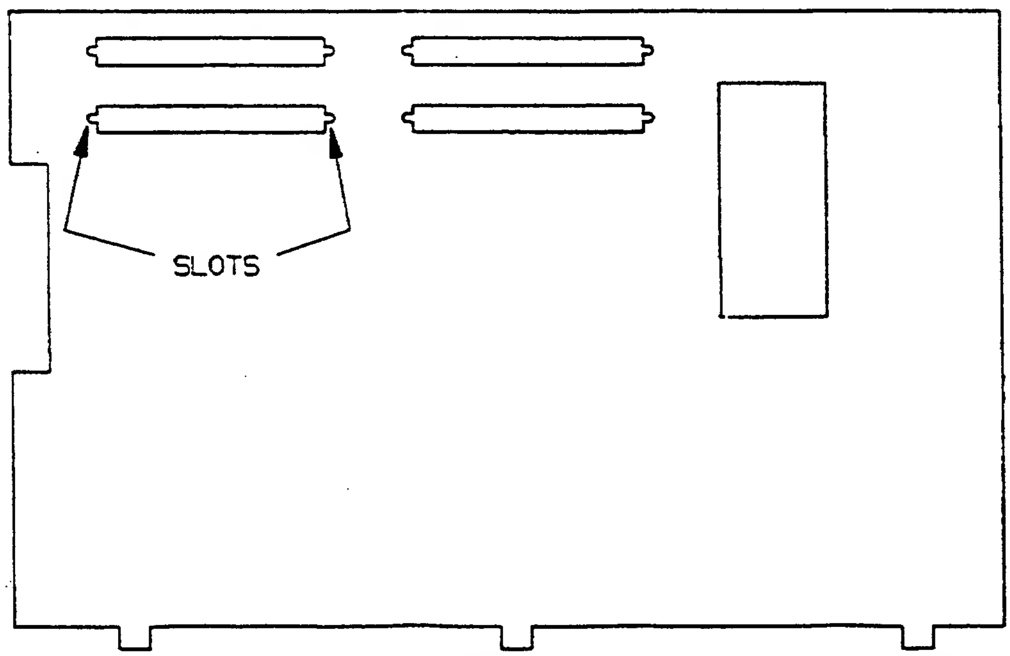


Figure 7-5. Pertec-compatible interface metal cover plate.

14. Bring the new interface close enough to the chassis to connect the 50-pin ribbon interface cable to the bottom of the interface PCA. The interface

assembly is positioned correctly when the three metal tabs on the interface assembly are pointing down.

15. Rotate the interface close enough to rear of the chassis so that the power connector (2-pin) can be connected to the right side of the interface.
16. Put the metal tabs at the bottom of the interface panel into the slots on the back panel of the drive. Rotate the interface assembly up flat against the rear panel.
17. Fasten the interface to the back panel with the two Torx™ screws.
18. On the Data Buffer PCA, connect a Jumper between the 2 test holes located above and to the right of the battery. (On the 07980-66504 PCA) use the two holes on the far right of the five holes at this location.)
19. Re-install the power cord.
20. Switch the drive On. FAIL 0 should appear in the display after a few seconds.
21. Switch the drive Off and remove the jumper installed in Step 18.
22. Switch the drive On.
23. Run TEST 129.
24. Run TEST 99 to set up the Preamp gain levels (do for 6250 cpi and 1600 cpi). Use a tape that is a TYPICAL brand and condition used by the customer. The tape should preferably NOT BE brand new, very old, or damaged.

25. Run Tests 105 and 106 on Option 800 NRZI Drives. Test 105 requires use of a Master Skew Tape (pn 9162-0027).
26. Reset the Error Log by setting CONF 0 to CLEAR.
27. Re-install any special customer configurations from the front panel.
28. Run TEST 2 to verify drive operation (a 600 ft tape is adequate).
29. Reconnect the interface cable to the drive.
30. "UP" the drive from the system console. (For HP systems only. For other systems, check the host manual.)
31. Do a system test/store and observe tape motion.

8

Troubleshooting and Diagnostics

Note The HP 7979A/S, HP 7980A/S, HP 7980SX/SX, and HP 88780A/B are collectively referred to as the "1/2-inch Tape Drives".

"XC/SX Only" indicates those tape drives that feature data compression.

8.1 Diagnostics Overview

The 1/2-inch Tape Drives contain very thorough built-in diagnostics. In addition, they maintain logs in non-volatile memory which provide error history to help in problem diagnosis.

Troubleshooting the drive is primarily done with the aid of selftests selected at the front panel. Various test categories are provided for a wide variety of troubleshooting demands. The test categories include the following:

The test number ranges are those reserved for tests of a particular category (not all numbers are used at this time).

Power On Test	General check of digital circuitry.
(0-36)	General drive function test sequences.
(38-39)	User-defined test sequence.
(40-49)	Kernal tests.
(50-59)	Processor communication tests.
(60-69)	Loopback tests.

(70-149)	Subsystem tests.
	(70-119) Drive Controller tests. (120-139) Buffer Controller tests. (140-149) Interface Controller tests.
(150-199)	Tape motion and Read/Write tests.
(200-255)	Host-specific tests/utilities.

Refer to Figure 8-1 for an illustration of the following troubleshooting information.

When a failure occurs, start with the Poweron Test, followed by general check sequence tests. These general tests initiate a sequence of exerciser and circuitry tests which verify most common drive functions. Passing the general sequence tests indicates that the digital circuitry and basic drive functions are working. This may also be a good time to check the error logs for the drive error history. Instructions for reading the error log appear in the "Errors" section of this chapter. When a sequence test detects a malfunction, the suspected failing component error code is displayed. The next step is to run the suggested selectable tests which exercise the suspected failing component and function.

If the sequence tests pass, interactive tests should be used to test the analog circuitry and electromechanical devices. These tests generally do not detect and report errors. They exercise an assembly and require the operator to watch for proper drive operation. To test the Tape Displacement Unit (TDU), for example, you would run Test 75 and watch for TDU movement.

With the exception of the Poweron sequence test, the running of tests requires operator intervention. Test *sequences*, however, do provide automatic branching to tests necessary for the sequence.

All tests can be initiated from the front panel. All tests, with the exception of tests which require operator intervention, can also be exercised remotely. When a failure is detected, an error message and isolation information is generated, logged and returned to the test initiator.

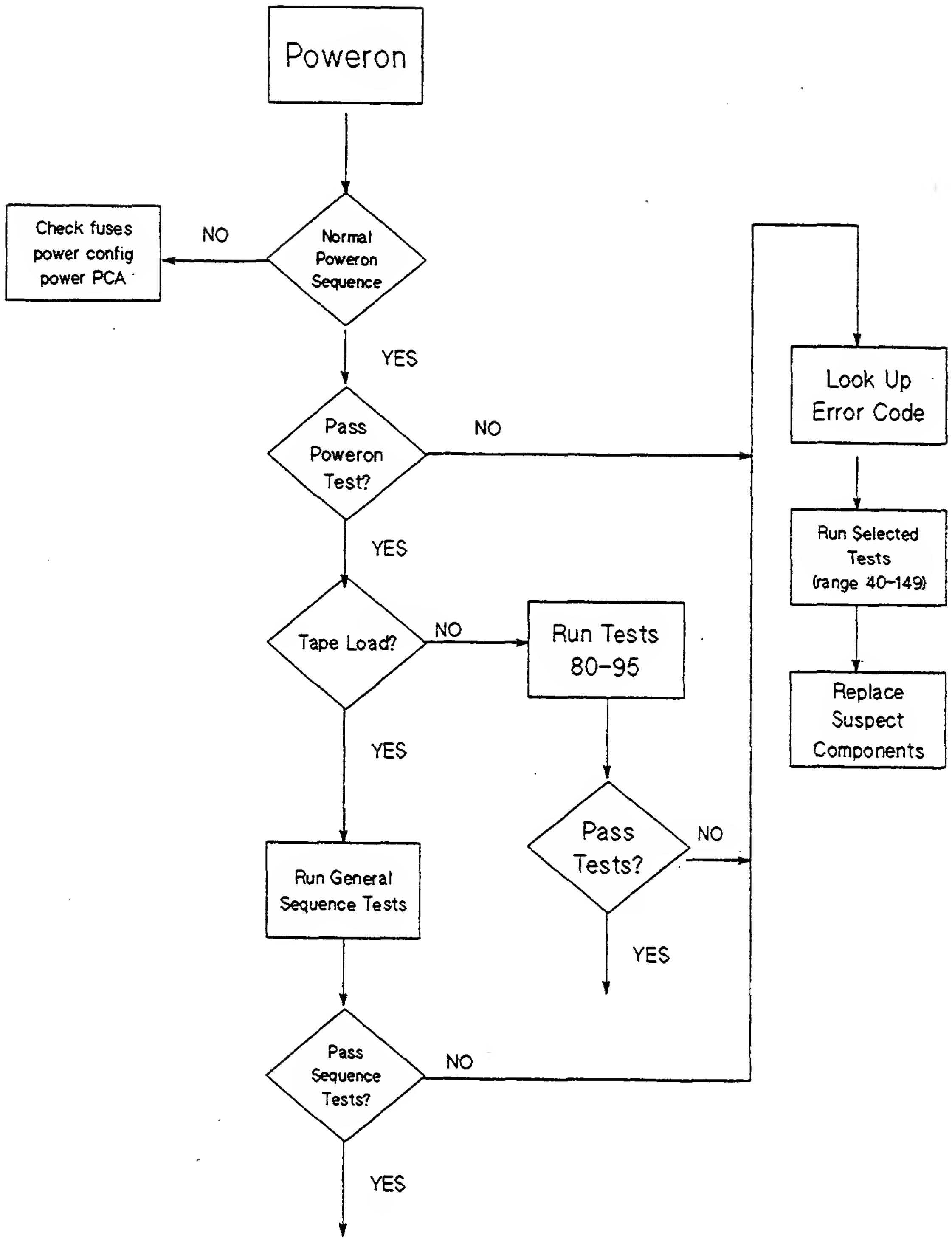


Figure 8-1. Troubleshooting Flowchart

8.2 Diagnostic Tests

The section includes the following information about diagnostic tests.

- Poweron test sequence explanation
- Runtime processing
  - Error logging
  - Error rate logging
  - Soft error warning
  - Odometer
- How to run a test
- Table of tests by test group
- Detailed description of each test

Poweron Test Sequence

When the machine is powered up, a sequence of tests are performed. The sequence order used when the drive is powered on is different than the Poweron sequence initiated on an already powered up drive.

At poweron, each of the processors is tested by the related kernel test. This testing takes place in parallel among all processors to minimize the poweron test time. Once all processors have completed individual tests, a Poweron handshake takes place between the processors. Finally, the drive controller is placed in control to execute the dual-port RAM and loopback tests.

Table 8-1. Poweron Test Sequence

Drive Controller	Buffer Controller	Interface Controller
Kernel tests	Kernel tests	Kernel tests
▼	▼	
Drive-specific tests	Buffer tests	Interface-specific tests
▼	▼	▼
Front panel lights	▼	▼
▶	Poweron handshake	◀
	▼	
	Complete dual-port RAM test	
	Loopback tests	

Errors detected during power-up are displayed on the front panel and stored in the error log held in non-volatile RAM.

Runtime Processing

During runtime certain functions are provided within the drive. They are mainly used to provide information for predictive diagnostics but also are used by some of the diagnostic tests.

Error Logging

Whenever a hard error occurs, the error is logged. This includes all errors which are detected by the drive while running a diagnostic which uses normal drive commands, as well as hardware failures during operation, and hard read/write failures resulting from unreadable or unwritable tape.

Error Rate Logging

For each read or write command that is received from the host, an entry is made in the current error rate log to account for the amount of read or write data in the transaction. The data from verify commands is included within the count since it requires that data be recovered, but data from move commands are not included even though readaheads would have recovered the data from the tape. Readaheads which are not passed to the host are not included. Whenever an error, either soft or hard, occurs it is added to current entry in the appropriate read or write accumulated error rate log. It is also added to the cumulative error log.

Soft Error Warning

As each command is logged, a check of the soft error rate is made for the current log entry. A threshold has been set at approximately 100 allowable errors per tape. The actual thresholds for the three densities are:

	Threshold	Minimum Transfer
NRZI	5 X E5	2 X E6
PE	5 X E5	2 X E6
GCR	2 X E6	8 X E6

A minimum transfer is required to prevent the warning from going off near the beginning of tape without a large enough sample. If these thresholds are exceeded, the message `CHECK` is displayed on the front panel in place of the `IDLE` message. The `CHECK` message DOES NOT indicate a loss of data. Cleaning the tape head typically will alleviate high soft error rate; however, it may indicate a more serious problem. The warning stays on as long as the threshold is exceeded.

Odometer

Each time the tape is unloaded, the amount of tape which passed over the head is accumulated with the odometer. This includes all tape motion including ramp up and ramp down lengths, as well as rewinds.

Running a Test

Caution Some tests will overwrite data on the tape.

Note Touching any of the parts inside the tape drive while a test is running can cause additional irrelevant errors.

To run a diagnostic test, follow these steps.

1. Switch on the drive and let the poweron test complete.
2. Load a write-enabled "scratch" tape.
3. Close the tape door.
4. After the drive positions the tape at BOT, take the drive OFFLINE (press [ONLINE], if necessary).
5. Press [OPTION]. TEST * appears in the display.
6. Press [ENTER].
7. Bring the test number you want into the display by pressing [NEXT] or [PREV].
8. Press [ENTER].
9. The display prompts `ONCE *`, asking you if you want the test to be run only once.

   If you would like to run the test more than once (perhaps checking for intermittent problems), use [NEXT] and [PREV] to display your other choices. Your other choices are: 10 times, 100 times, 1000 times, or LOOP (run continuously until [RESET] is pressed).
10. Press [ENTER] to run the test.

    The drive displays `RUN test number`, indicating which individual test in the sequence is running.

Note

To abort a test, press (RESET) while the test is running. Press (RESET) one more time to return to the Option Select level (TEST * appears in the display).

11. When the test is complete, either `PASS test number` or `FAIL test number` is displayed.

    If the test passed and you want to repeat the test or to select another test, press (ENTER) or (RESET). The display will return to the level that displays the test number.

    If you want to select the same test, press (ENTER) and then repeat Steps 8 and 9.

    If you want select another test, use the (NEXT) and (PREV) keys.

12. If the test fails, press (ENTER) to display the error that caused the failure.

    Press (RESET) three times to completely exit through the test selection and Option Select levels.

13. Press (OPTION) or (RESET) to leave Option Mode.

Test Reference Table

Table 8-2. Diagnostic Tests

Test No.	Test Description	Test Type	μP	P/O	Test Param	Used in Tests	FRUs Tested See Table 8-3
Sequence Tests							
0	Poweron Test	S[1]	A		–	1	Refer to individual tests.
1	General Checkout	S	A[2]	–	–		Refer to individual tests.
2	Wellness Test	S	D,B	–	–	1	Refer to individual tests.
3	Initialize Error Rate	S	B	–	–		Refer to individual tests.
4	Error Rate	S	D,B	–	–		Refer to individual tests.
5	NRZI Error Rate	S	D,B	–	–		Refer to individual tests.
9	Multiprocessor	S	D,B,I	P[3]	–	0	Refer to individual tests.
11	Dual-Port RAM	S	D,B,I	–	–	9	Refer to individual tests.
12	Loopback Isolation	S	D,B,I	–	–		Refer to individual tests.

1 Test Types are: C = Check, E = Exerciser, S = Sequence, T = Test, X = Command Reference

2 Processor Types are: A = All, B = Buffer, D = Drive, F = Front Panel, and I = Interface.

3 P = Used at Poweron

Table 8-2. Diagnostic Tests (continued)

Test No.	Test Description	Test Type	μP	P/O	Test Param	Used in Tests	FRUs Tested See Table 8-3
13	Drive Controller Poweron	S	A	P	–	0	Refer to individual tests.
14	Buffer Controller Poweron	S	A	P	–	0, 19	Refer to individual tests.
15	Interface Poweron	S	A	P	–	0, 20	Refer to individual tests.
17	Servo/Motor Drive Elec.	S	D	–	–	13	Refer to individual tests.
18	Servo/Motor Drive Check	S	D		–		Refer to individual tests.
19	Buffer Hardware	S	B		–	12	Refer to individual tests.
20	Interface-Spec. Hardware	S	I		–	12	Refer to individual tests.
38	Enter User-Defined Seq.	S					User defined
39	Run User-Defined Seq.	S					User defined

Table 8-2. Diagnostic Tests (continued)

Test No.	Test Description	Test Type	μP	P/O	Test Param	Used in Tests	FRUs Tested See Table 8-3
Kernal Tests							
40	Microprocessor Test	T	A	P	1	0,1,13,14,15	Dc,Db,Gi
41	ROM Checksum	T	A	P	1	0,1,13,14,15	Dc,Db,Gi
42	Destructive RAM	T	D,I	P	-		Dc,Gi
43	Non-destructive RAM	T	A	P	1	0,1,13,14,15	Dc,Db,Gi
44	Complete RAM	T	A	-	1		Dc,Db,Gi
45	Connective Test	T	A	P	1	0,1,13,14,15	Ic,Sc,Fc,Es, Ba,Mc
46	Destructive DPR	T	D,B	P	-		Dc,Db
48	Non-volatile RAM	T	B	P	-	0,1,14	Db
49	Timer Circuitry	T	D	P	-	0,1,19	Dc

Table 8-2. Diagnostic Tests (continued)

Test No.	Test Description	Test Type	μP	P/O	Test Param	Used in Tests	FRUs Tested See Table 8-3
Processor Communication Tests							
50	Onboard DPR Test	T	D,B	P	1	0,1,9,11	Dc,Db,Gi
51	Offboard DPR Test	T	B,I	P	1	0,1,9,11	Dc,Db,Gi
52	DPR Collision Test	T	A	P	1	0,1,9,11	Dc,Db,Gi
53	Sub DPR Interrupt	T	D,B	P	1	0,1,9,11	Dc,Db,Gi
54	Master DPR Interrupt	T	B,I	P	1	0,1,9,11	Dc,Db,Gi
Loopback Tests							
60	Interface Loopback	T	I	P	1	0,1,9,12	Gi
61	Buffer Init. Loopback	T	B	P	2	0,1,9,12	Db,Fm
62	Drive Init. Loopback	T	D	P	1	0,1,9,12	Dc,Fm,Rw
63	Digital Loopback Exer	E	D	-	2		Dc,Fm,Rw
64	Drive Init	T	D	-	1		Hd,Dc,Fm,Rc,
	Analog Loop						Wc,Rw
65	Analog	E	D	-	1		Hd,Dc,Fm,Rc,
	Loopback Exer						Wc,Rw

Table 8-2. Diagnostic Tests (continued)

Test No.	Test Description	Test Type	μP	P/O	Test Param	Used in Tests	FRUs Tested See Table 8-3
Drive Controller Tests							
70	Front Panel Light Show	C	F	P	-	0,1,13	Fp
71	Front Panel Button Chk	C	F	-	-		Fp
72	Front Panel Message Chk	C	F	-	-		Fp
75	TDU Test	T	D	-	-	1	Td
76	DAC Test	T	D	P	-	0,1,13,17	Dc
77	Tachometer Test	T	D	P	-	0,1,13,17	Dc
78	ADC Test	T	D	P	-	0,1,13,17	Dc
80	Motor Drive Loopback	T	D	P	-	0,1,13,17	Dc,Md
81	45 VoltPower Supply	T	D	P	-	0,1,13,17	Md
82	Position Counter Test	T	D	P	-	0,1,13,17	Dc,Se
84	Tension Shutdown Check	C	D	-	-		Ba,Es
85	Tension Sensor Check	C	D	-	-		Ba,Es
86	Speed Encoder Check	C	D	-	-		Se

Table 8-2. Diagnostic Tests (continued)

Test No.	Test Description	Test Type	μP	P/O	Test Param	Used in Tests	FRUs Tested See Table 8-3
87	Tape in Path Sensor Check	C	D	-	-		Sb
88	Door Sensor Check	C	D	-	-		Sb,Dc
89	Reel Encoders/Write	C	D	-	-		Hl,Sb
	Enable Ring Sensor						
90	TDU Functional Check	C	D	-	-		Td
91	Hub Lock Check	C	D	-	-		Hl,Md
92	Hub Unlock Check	C	D	-	-		Hl,Md
93	Load Fan Check	C	D	-	-		FAN
94	EOT/BOT Sensor Check	C	D	-	-		Es
95	Servo Performance Test	T	D	-	-	1,18	Dc,Md
96	Servo Reposition Exer	E	D	-	2	18	
97	Servo Close Loops Test	T	D	-	-		Dc,Ba
98	Read Ch Gain Profile	C	D	-	2		

Table 8-2. Diagnostic Tests (continued)

Test No.	Test Description	Test Type	μP	P/O	Test Param	Used in Tests	FRUs Tested See Table 8-3
99	Auto Calibration Exer	E	D	-	-		
100	Erase Tape Test	T	D	-	1		
101	Write Electronics Exer	E	D	-	1		
102	Read Electronics Exer	E	D	-	1		
103	Read Reverse Exer	E	D	-	1		
104	Read Crosstalk Exer	E	D	-	1		
105	Read Skew Calibration	T	D	-	1		
106	Write Skew Calibration	T	D	-	1		
107	NRZI Skew Value Disp	C	D	-	1		
108	Current Gain Profile	C	D	-	1		
109	NRZI Dynamic Skew	T	D	-	-		
110	Tape Pack Conditioner	E	D	-	-		

Table 8-2. Diagnostic Tests (continued)

Test No.	Test Description	Test Type	μP	P/O	Test Param	Used in Tests	FRUs Tested See Table 8-3
Buffer Controller Tests							
120	Buffer Register Test	T	B	P	-	0,1,12,14,19	Db
121	Buffer Function Test	T	B	P	-	0,1,12,14,19	Db
122	Buffer RAM Test	T	B	P	-	0,1,12,14,19	Db
128	Dump NV RAM to Tape	X	B	-	-		
129	Load NV RAM from Tape	X	B	-	-		

Table 8-2. Diagnostic Tests (continued)

Test No.	Test Description	Test Type	μP	P/O	Test Param	Used in Tests	FRUs Tested See Table 8-3
Data Compression Tests							
130	Data Comp Register Test	T	B	P	-	0,1,12,14,19	Db (FRU 24 only)
131	Data Comp Functionality	T	B	P	1	0,1,12,14,19	Db (FRU 24 only)
132	Data Comp Ram Test	T	B	P	-	0,1,12,14,19	Db (FRU 24 only)
133	Data Comp Extended Functionality	T	B	P	1	0,1,12,14,19	Db (FRU 24 only)
Interface Controller Tests							
140	HPIB Controller Test	T	I	P	-	0,1,12,15,20	Hp
140	SCSI Controller Test	T	I	P	-	0,1,12,15,20	Sd,Ss
141	Onboard Hardware Tests	T	I	P	-	0,1,12,15,20	Hp,Sd,Ss,Pt

Table 8-2. Diagnostic Tests (continued)

Test No.	Test Description	Test Type	µP	P/O	Test Param	Used in Tests	FRUs Tested See Table 8-3
Execute Drive Commands							
150	Write Density ID	X	D	-	1	1,2,3,4	
151	Write Test Record	X	D	-	1		
152	Write Tape Mark	X	D	-	-	1,2,3,4	
153	Write Gap	X	D	-	1		
160	Verify Record	X	D	-	1		
161	Forward Space Block	X	D	-	-		
162	Backspace Block	X	D	-	-		
163	Forward Space File	X	D	-	-		
164	Backspace File	X	D	-	-		
165	Load Tape	X	D	-	-	1,2,3,4,18	
166	Rewind	X	D	-	-	1,2,3,4,18	
167	Unload Tape	X	D	-	1	18	
170	Write Tape Mark to Buff	X	B	-	-		

Table 8-2. Diagnostic Tests (continued)

Test No.	Test Description	Test Type	μP	P/O	Test Param	Used in Tests	FRUs Tested See Table 8-3
171	Create Record in Buff	X	B	-	2	1,2,3,4	
172	Write Buffer to Tape	X	B	-	1	1,2,3,4	
173	Read from Tape to Buff	X	B	-	1	1,2,3,4	
174	Clear Data Buffer	X	B	-	-	1,2,3,4	
175	Initialize Cumul. Log	X	B	-	-	3	
176	Buff Write Tape Mark	X	B	-	-		
177	Buffer Write Density	X	B	-	-		

Field Replaceable Units

Here is a table that lists all of the FRUs and all tests that can detect problems with a particular FRU.

Table 8-3. Diagnostic Tests and Field Replaceable Units

No.	FRU	FRU Name	Tests Applicable to FRU
01	Rw	Read/Write/PLL	62, 63, 64, 65, 98, 100
02	Fm	Formatter	61, 62, 63, 64, 65
03	Dc	Drive Controller	40-44, 46, 49, 50-54, 62-65, 76-80, 82, 88, 95, 97
04	Db	Data Buffer	40, 41, 43, 44, 46, 48, 50-54, 61, 120-122
05	Md	Motor Drive/Power Supply	80, 81, 91, 95
06	Gi	Generic (any) Interface	40-44, 50-54, 60
07	Hp	HPIB Interface	40-44, 50-54, 60, 140, 141
08	Fp	Front Panel	70-72
09	Sb	Supply Reel Sensor PCB	87-89
10,16,36	Sd	SCSI Differential Interface	40-44, 50-54, 60, 140, 141
11,15,35	Ss	SCSI Single-ended Interface	40-44, 50-54, 60, 140, 141
12,22	Pt	Pertec-compatible Interface	40-44, 50-54, 60, 140, 141
13	Dc	7979 Drive Controller	40-44, 46, 49, 50-54, 62-65, 76-80, 82, 88, 95, 97
14	Db	Data Buffer Non XC	40, 41, 43, 44, 46, 48, 50-54, 61, 120-122
21	Fm+Rw	Formatter/R/W/PLL	61-64, 66, 98, 100
24	Db	Data Buffer 7980XC/SX	40, 41, 43, 44, 46, 48, 50-54, 61, 120-122, 130-133
31	+NRZI Fm+Rw	Formatter/R/W/PLL	61-64, 66, 98, 100, 105, 106
34	Db	Data Buffer w/1Mb RAM	40, 41, 43, 44, 46, 48, 50-54, 61, 120-122

Table 8-3.
Diagnostic Tests and Field Replaceable Units (continued)

No.	FRU	FRU Name	Tests Applicable to FRU
Assemblies			
40	Es	EOT/BOT Sensors	45, 84, 85, 94
41	Se	Speed Encoder	82, 86
42	Hd	Head Assembly	64, 65, 100
44	Hl	Hub Lock	89, 91, 92
45	Ba	Buffer Arm	45, 84, 85, 97
51	Td	Tape Displacement Unit	75, 90
Cables			
62	Sc	Speed Sensor Cable	45
64	Fc	Front Panel Cable	45
65	Mc	Motor Cable	45
66	Sc	Slave Connector	45
67	Ic	Interface Cable	45
70	Sv	Servo Cable	
71	Rc	Read Cable	64, 65
72	Wc	Write Cable	64, 65
Other			
50	Mo	Motors	Evaluate by inspection.
—	Ds	Door Solenoid	88
—	—	Fan	Evaluate by inspection.
—	—	Mother Board/card cage	Evaluate by insepction.
—	—	Hubs	Evaluate by inspection.
—	—	Transformer	Evaluate by inspection.

Test Descriptions

Refer to Table 8-2 for a concise chart of tests.

The three classes of diagnostic tests are:

Interactive Checks	These require operator intervention, and give immediate front panel response indicating the results of the intervention. Checks continue to operate until the reset button is pressed, and always return a diagnostic result of passed. The loop count parameter is ignored during these tests.
Exercisers	These tests cause the drive to perform a specific function to be observed or monitored by the operator. They do not return an error unless an invalid setup prevents the test from operating.
Tests	These tests are written such that the drive can detect a failure. A `PASS` or `FAIL` is returned on test completion.
Command Execution	The Drive Command Execution tests many of the read/write and tape handling commands, either individually from the front panel or as part of a sequence. Errors that occur while executing these commands use the runtime error set. No isolation or suspected FRUs are indicated in the error message.

Sequences may combine both exercisers and tests, but will typically not include interactive checks because of their need for operator intervention.

All four test classes are described in the following sections. Additional parameters or special requirements, where necessary, are included.

Sequence Tests (0 - 39)

This group does not contain individual tests but rather sequences of tests in the range of Tests 40 through 199. Sequences may be used as a general test of the drive, or as a drive exerciser. When a sequence is selected, The drive will execute the tests in the sequence until an error occurs, or until the sequence successfully completes.

Test 0 - Power On

Checks out all digital data paths and normal machine operation. This sequence runs tests that are similar to those normally run at poweron. The tests for each controller are run serially here rather than in parallel as in actual powerup.

Sequence Order:

13 - Drive Controller Poweron sequence

14 - Buffer Controller Poweron sequence

15 - Interface Poweron sequence

9 - Multiprocessor Sequence

Test 1 - General Checkout (scratch tape required)

This test performs a complete machine checkout. It runs all poweron tests, then loads a tape and checks out all sensors. It then runs the tests in the multiprocessor, sensor, and wellness sequences.

Sequence Order:

0 - Power On

165 - Load Tape

75 - TDU Test

95 - Servo Performance Test

2 - Wellness Test

Test 2 - Wellness
(scratch tape required)

This test checks out the general read/write capability of the 1/2-inch Tape Drive. The sequence includes the tests necessary to write a GCR tape, rewind and read the tape, rewind, write the tape in PE, rewind and read the PE tape, rewind, write the tape in NRZI (if available), rewind and read the NRZI tape, then rewind.

During the write process, the (ENTER) key causes the write to end early so that the entire tape is not written. The subsequent read pass will only read as far as the write pass had written.

Sequence Order:

Test Number	Description	Param A	Param B
165	Load Tape		
174	Clear Data Buffer		
171	Create Record in Buffer	1, all ones	4K
171	Create Record in Buffer	2, alternating	16K
171	Create Record in Buffer	3, rotating	32K
150[1]	Write Density ID	6250	
177[2]	Write Density ID	6250	
172[1]	Write Buffer to Tape	1, LOOP *	
176	Write Tape Mark		
176	Write Tape Mark		
166	Rewind		
173	Read From Tape to Buffer	0, LOOP *	
166	Rewind		
174	Clear Data Buffer		
171	Create Record in Buffer	1, all ones	4K
171	Create Record in Buffer	2, alternating	16K
171	Create Record in Buffer	3, rotating	32K
150[1]	Write Density ID	1600	
177[2]	Write Density ID	1600	
172	Write Buffer to Tape	1, LOOP *	
176	Write Tape Mark		
176	Write Tape Mark		
166	Rewind		

1 FRU 4 Buffer

2 FRU 14, 24 or 34 Buffer

Test Number	Description	Param A	Param B
173	Read From Tape to Buffer	0	
166	Rewind		
174	Clear Data Buffer		
171	Create Record in Buffer	1, all ones	4K
171	Create Record in Buffer	2, alternating	16K
171	Create Record in Buffer	3, rotating	32K
177	Write Density ID	800	
172	Write Buffer to Tape	1, LOOP *	
176	Write Tape Mark		
176	Write Tape Mark		
166	Rewind		
173	Read From Tape to Buffer	0, LOOP *	
166	Rewind		
174	Clear Data Buffer		

Test 3 - Initialize Error Rate Sequence

Sequence 3 initializes the cumulative error rate logs, Info 3, 4 and 5.

Sequence Order:

175 - Initialize cumulative logs

Test 4 - Error Rate Sequence (scratch tape required)

Sequence 4 writes a tape in GCR, rewinds and reads it, then performs the same operations in PE and NRZI (if available). While the sequence runs, read/write errors are recorded in the cumulative error rate log. The error rate results are viewed in the cumulative error rate logs from INFO 3, 4, and 5. Error rate results are accumulated until sequence 3 is used to initialize the log.

The error rate sequence operates very similar to the wellness test but differs in that hard read and write error do not terminate the error rate test. Hard errors are only logged.

Sequence Order:

Test Number	Description	Param A	Param B
165	Load Tape		
174	Clear Data Buffer		
171	Create Record in Buffer	1, all ones	4K
171	Create Record in Buffer	2, alternating	16K
171	Create Record in Buffer	3, rotating	32K
150[1]	Write Density ID	6250	
177[2]	Write Density ID	6250	
172	Write Buffer to Tape	5, LOOP *	
176	Write Tape Mark		
176	Write Tape Mark		
166	Rewind		
173	Read From Tape to Buffer	4, LOOP *	
166	Rewind		
174	Clear Data Buffer		

1 FRU 4 Buffer

2 FRU 14. 24, or 34 Buffer

Test Number	Description	Param A	Param B
171	Create Record in Buffer	1, all ones	4K
171	Create Record in Buffer	2, alternating	16K
171	Create Record in Buffer	3, rotating	32K
150[3]	Write Density ID	1600	
177[4]	Write Density ID	1600	
172	Write Buffer to Tape	5, LOOP *	
176	Write Tape Mark		
176	Write Tape Mark		
166	Rewind		
173	Read From Tape to Buffer	4, LOOP *	
166	Rewind		
174	Clear Data Buffer		
171	Create Record in Buffer	1, all ones	4K
171	Create Record in Buffer	2, alternating	16K
171	Create Record in Buffer	3, rotating	32K
177	Write Density ID	800	
172	Write Buffer to Tape	5, LOOP *	
176	Write Tape Mark		
176	Write Tape Mark		
166	Rewind		
173	Read From Tape to Buffer	4, LOOP *	
166	Rewind		
174	Clear Data Buffer		3 FRU 4 Buffer 4 FRU 14 Buffer

Test 5 - NRZI Error Rate Sequence

(scratch tape required)

Sequence 5 writes a tape in NRZI then rewinds and reads it. While the sequence runs, read/write errors are recorded in the PE cumulative error rate log. The error rate results are viewed in the cumulative error rate logs, INFO 4 and 5. Error rate results are accumulated until sequence 3 is used to initialize the log.

The NRZI error rate sequence operates very similar to the wellness test but differs in that hard read and write errors do not terminate the error rate test. Hard errors are only logged.

Sequence Order:

Test Number	Description	Param A	Param B
165	Load Tape		
174	Clear Data Buffer		
171	Create Record in Buffer	1, all ones	4K
171	Create Record in Buffer	2, alternating	16K
171	Create Record in Buffer	3, rotating	32K
177	Buffer Write Density ID	800	
172	Write Buffer to Tape	5, LOOP *	
176	Write Tape Mark		
176	Write Tape Mark		
166	Rewind		
173	Read From Tape to Buffer	4, LOOP *	
166	Rewind		
174	Clear Data Buffer		

Test 9 - Multiprocessor Sequence

This sequence will execute all multiprocessor tests to check out the communication between processors, the message bus, and data transfer paths. It will normally be called after each processor has executed its individual poweron sequence and established communications at powerup.

Sequence Order:

11 - Dual-Port RAM Test Sequence

62 - Formatter Initiated Loopback Test

61 - Buffer Initiated Loopback Test (Param B = 3)

60 - Interface Initiated Loopback Test

Test 11 - Dual-Port RAM Sequence

This sequence will perform all tests on the dual-port RAM between all target processors.

Sequence Order:

Test Number	Description	Param A
50	DPR On Board Test	3, DC
51	DPR Off Board Test	4, BC
50	DPR On Board Test	4, BC
51	DPR Off Board Test	6, IF
53	DPR Interrupt Test	4, DC to BC
54	DPR Interrupt Test	3, BC to DC
54	DPR Interrupt Test	4, IF to BC
52	DPR Collision Test	3, BC to DC
52	DPR Collision Test	4, IF to BC

Test 12 - Loopback Isolation Sequence

This sequence will execute all Interface, Buffer initiated, and Formatter initiated loopback isolation sequences. All hardware areas used by loopbacks will be checked out. Each loopback test is stepped through and a loopback problem should be isolated. Each test will be executed with a loopback check number (Param A) of zero and will run all loopback checks.

Sequence Order:

62 - Formatter Initiated Loopback test

19 - Buffer Hardware Sequence

61 - Buffer Initiated Loopback test (Param B 3, rotating)

20 - Interface Specific Hardware Sequence

60 - Interface Loopback Test

Test 13 - Drive Controller Poweron Test Sequence

This sequence will be executed by the drive controller at powerup to check out all paths and operation of the servo and motor drive circuitry.

Sequence Order:

41 - Rom Checksum

40 - Processor Test

43 - Non-Destructive RAM Test

45 - Connectivity Test

49 - Timer Circuitry Test

70 - Front Panel Test

17 - Servo/Motor Drive Electronics Sequence

Test 14 - Buffer Controller Poweron Test Sequence

This sequence will be executed by the buffer controller at powerup and will check out all paths and operation of the buffer circuitry.

Sequence Order:

41 - Rom Checksum

40 - Processor Test

48 - Non-volatile RAM Checksum

43 - Non-destructive RAM Test

45 - Connectivity Test

19 - Buffer Hardware Sequence

Test 15 - Interface Poweron Test Sequence

This sequence will be executed by the interface controller at powerup and will check out all paths and operation of the specific interface.

Sequence Order:

41 - Rom Checksum

40 - Processor Test

43 - Non-Destructive RAM Test

45 - Connectivity Test

20 - Interface Specific Hardware Sequence

Test 17 - Servo/Motor Drive Electronics Sequence

(no scratch tape)

This sequence will check out the operation of the servo and motor drive circuitry. These sequence tests are non-interactive.

Sequence Order:

78 - ADC Test

76 - DAC Test

82 - QDC Test

77 - Tachometer Test

81 - 48 Volt PSU Test

80 - Motor Drive Loopback

Test 18 - Servo/Motor Drive Checkout Sequence

(scratch tape required)

Sequence Order:

165 - Load Tape 95 - Servo Performance Test 96 - Servo Repositioning Test

166 - Rewind Tape

167 - Unload Tape

Test 19 - Buffer Hardware Sequence

This sequence will checkout the data path and operation of the data buffer registers and RAM. It will isolate any problems specific to the data buffer.

Sequence Order:

120 - Buffer Register Test

121 - Buffer Function Test

122 - Buffer RAM Test

130[1] - Data Compression Register Test

131[1] - Data Compression RAM Test

132[1] - Data Compression RAM Test

[1]XC/SX product only

Test 20 - Interface-Specific Hardware Sequence

This sequence will run through all of the interface specific hardware tests.

Sequence Order:

140 - Interface Specific Test 1

141 - Interface Specific Test 2

User-Defined Sequence (Tests 38 - 39)

A sequence consisting of up to twenty tests may be defined by the user during runtime. The sequence entries may consist of any existing tests or sequences. The sequence is defined by invoking Test 38 and entering the test or sequence numbers in the correct order. The user-defined sequence is run using Test 39. The current definition remains in NV-RAM until another sequence is defined using Test 38.

Test 38 - Enter Used-Defined Sequence. This test will allow a user-defined sequence to be entered. When tests are run while defining Test 39, they will complete with a `SEQ 39` message immediately, instead of the normal `PASS` or `FAIL`. Running Test 38 a second time terminates the sequence of definition mode.

Test 39 - Run User-Defined Sequence. This test will run the current user-defined sequence. If Test 39 is currently being defined, this test completes the sequence definition and then runs the test.

Kernal Tests (40 - 49)

All kernal tests and certain multiprocessor tests require a Target processor parameter. These tests are common to more than one processor and as such the processor must be specified. The possibilities are as follows:

Target Processor

0 - All processors
3 - Drive controller
4 - Buffer controller
6 - Interface controller
7 - HPIB Interface controller
10 - SCSI differential interface controller
11 - SCSI single ended interface controller
12 - Pertec-compatible interface controller

The default processor is "All processors." With all processors set, each processor which has the test defined, will execute the test, beginning with the interface controller, and ending with the drive controller.

Test 40 - Microprocessor Operation

(param A - processor (0,3,4,6))

A functional check of the microprocessor is performed.

Test 41 - ROM Checksum

(param A - processor (0,3,4,6))

A checksum verification of the ROM is performed.

Test 42 - Destructive RAM Test

Volatile RAM is tested, checking for data acceptance and retention. The test insures that writing to one location has no affect on other locations. This test is destructive and as such will only run at poweron.

Test 43 - Non-Destructive RAM Test

(param A - processor (0,3,4,6))

RAM is tested, checking for data acceptance and retention. The test is non-destructive. This test is used at poweron for non-volatile RAM and while running the poweron test sequence for all RAM areas.

Test 44 - Complete RAM Test

(param A - processor (0, 3, 4, 6))

RAM is fully tested for data acceptance and retention. The test also insures that no memory cells affect other cells within the RAM. This test is non-destructive and may be used without powercycling the drive, but does require extended times to run.

Param A	Processor	Time Required for Test
3	Drive controller	17 minutes
4	Buffer controller	72 minutes (504 buffer) 1.5 minutes (514/524 buffer) 3.0 minutes (534 buffer)
6	Interface controller	4 minutes HP-IB and PERTEC 17 minutes SCSI
0	All of above	22.5 to 106 depending on buffer and interface frus (see above).

Test 45 - Connectivity Test

(param A - processor (0,3,4,6))

All connectors are checked for proper connectivity.

Test 46 - Destructive Dual-Port RAM Test

The dual-port RAM is tested using the destructive RAM test. This test is destructive and is only run at poweron. It is NOT accessible from the front panel.

Test 48 - Non-Volatile RAM Checkout

A RAM test and checksum verification of the controlled portion of non-volatile RAM is performed.

Test 49 - Timer Circuitry

The PTM is checked for proper counting. The oscillator is used to verify the STS has the proper period.

Processor Communication Tests (50 - 59)

Processor communication tests verify the dual-port RAM functions through which all inter-processor command communications take place.

Test 50 - Onboard DPR

(param A - processor (0, 3, or 4))

This test allows the DPR to be checked out from the subordinate side. The test performs a walking ones and zeros test in a non-destructive manner. All of the RAM may be accessed for checking with the exception of the master interrupt location.

Test 51 - Offboard DPR

(param A - processor (0, 4, or 6))

This test allows the DPR to be checked out from the master side. The test performs a walking ones and zeros test in a non-destructive manner. All of the RAM may be accessed for checking with the exception of the subordinate interrupt location.

Test 52 - DPR Collision

(param A - processor (0, 3, or 4))

This test checks DPR arbitration by creating read/write collisions at the DPR. The two processors then pass incrementing information back and forth through the diag message area (DPR location 084H).

Test 53 - Subordinate DPR Interrupt

(param A - processor (0, 4, or 6))

This test verifies the ability of the master to be interrupted by the subordinate through the DPR. The test is initiated by the target processor sending a multiprocessor command with the parameter set to "subordinate interrupt." The receiving processor will write the interrupt test value to the interrupt location of the DPR then report on the command.

Test 54 - Master DPR Interrupt

(param A - processor (0, 3, or 4))

This test verifies the ability of the subordinate to be interrupted by master through the DPR. The test is initiated by the target processor sending a multi-processor command with the parameter set to "master interrupt". The receiving processor will write the interrupt test value to the interrupt location of the DPR then report on the command.

Loopback Tests (60 - 69)

Loopback tests perform data transfers between subsystems.

Test 60 - Interface Loopback

(param A - loopback check number)

The interface uses manual CCL commands to communicate with the data buffer. Test will pass if expected result occurs.

Parameter A indicates the extent of the test:

Param A	Loopback Check	Expected Result
0	Run all loopback checks from 1 thru 3	
1	Loopback correct data	No error
2	Data to buffer with a parity error (This test option is not available on HP-IB interface)	Data parity error
3	Data from buffer with a parity error	Data parity error

Test 61 - Buffer Initiated Loopback

(param A - loopback type) (param B - data pattern)

Data is generated within the buffer then looped through the formatter using the multi-processor loopback command. Parameter A indicates the extent of the test:

Param A	Loopback Check
0	Run all loopback checks from 1 thru 5
1	Correct PE data
2	Correct GCR data
3	Correct GCR data underrun (PE for 7979 drives)
4	Correct GCR data overrun (PE for 7979 drives)
5	GCR data with a parity error (PE for 7979 drives)
6	Correct NRZI data

Param B	Data Pattern
0	All zeros
1	All ones
2	Alternating ones and zeros
3	Rotating 0 - 255
4	Pseudo random

Test 62 - Drive Initiated Digital Loopback

(param A - loopback block type)

Loopback data or a write pattern is generated by the drive controller and passed through the formatters.

Number	Loopback Block Type
0	Run all block types form 1 thru 16
1	1600 PE data block
2	1600 PE data block with 1 track in error
3	1600 PE density ID
4	1600 PE tape mark
5	1600 PE gap
6	6250 GCR data block
7	6250 GCR data block with 1 track in error
8	6250 GCR data block with 2 tracks in error
9	6250 GCR density ID
10	6250 GCR ARA burst
11	6250 GCR ARA ID
12	6250 GCR tape mark
13	6250 GCR gap
14	800 NRZI data block
15	800 NRZI tape mark
16	800 NRZI gap

Test 63 - Digital Loopback Exerciser

(param A - density) (param B - tracks selector)

Digital loop back is performed using a data block in the selected density with the selected tracks turned off. Tracks selector is in the form of 'XY' where X and Y are combinations of two tracks to disable. Tracks may be specified as 1 through 9 with 0 indicating no tracks.

Tests 64/65 Because this test does not do retries, tape defects will cause errors when running this test.

Test 64 - Drive Initiated Analog Loopback

(param A - loopback block type) (requires scratch tape)

Loopback data or a write pattern is generated by the drive controller and passed through the formatters and the tape. Loopback block type is defined in Test 62.

Test 65 - Analog Loopback Exerciser

(param A - density) (param B - tracks selector)(Requires scratch tape.)

Analog loop back is performed using a data block in the selected density with the selected tracks turned off. Tracks selector is in the form of 'XY' where X and Y are combinations of two tracks to disable. Tracks may be specified as 1 thru 9 with 0 indicating no tracks.

Drive Controller Tests (70 - 119)

Test 70 - Front Panel Light Show

Test 71 - Front Panel Button Check

(interactive test) Displays the name of each button for one second after they are pressed. The test is terminated by pressing (RESET) twice.

Test 72 - Front Panel Message Check

(interactive test)

This test displays all the front panel messages. The front panel buttons are defined as follows for the duration of the test:

(NEXT)	Selects the next message to be displayed, cycling through all the messages for the current language.
(PREV)	Selects the previous message to be displayed, cycling through all the messages for the current language.
(OPTION)	Selects the next language, cycling through all the languages (English, German, French, Spanish). The odometer indicates the current language (0=English, 1=German, 2=French, 3=Spanish).
(ONLINE)	Resets the message pointer back to the first message.
(ENTER) or (RESET)	Terminates the test.

Test 75 - TDU

(scratch tape required)

Performs a write/read test with TDU engages and disengages to verify proper TDU operation. The scratch tape must have a PE or GCR density ID and be positioned at BOT.

Test 76 - DAC

(tape must be unloaded)

Values are written to the DACs and checked with an A/D converter.

Test 77 - Tachometer

(tape must be unloaded)

The tach circuit at the speed encoder inputs is simulated. Proper speed translation and the A/D converter are checked.

Moving the tape speed sensor durng this test may caue the test to fail with Error 356.

Test 78 - ADC

Test the A/D converter for proper operation.

Test 80 - Motor Drive Loopback

(tape must be unloaded)

Values are written to the motor DAC and read back at the A/D converter.

Positioning the tape buffer arm past the over-tension shutdown point will cause this test to fail with Error 353 or 354.

Test 81 - 48-Volt Power Supply

The A/D converter is read for the 48 volt PSU

Test 82 - Position Counter

(tape must be unloaded)

CHAN-A and CHAN-B bits are toggled on the QDC. Proper counts are checked.

Moving the tape speed sensor during this test may cause the test to fail with Error 355.

Test 84 - Tension Shutdown Check

(interactive test, tape must be unloaded)

As the tester moves the tension arm (buffer arm), the front panel displays * when a tension shutdown limit is reached.

Test 85 - Tension Sensor Check

(interactive test)

The front panel displays the tension arm value obtained from the A/D converter in the range of 0 - 255. The midpoint of the readings (seen when no tension arm is installed) is approximately 122.

Test 86 - Speed Encoder Check

(interactive test)

As the operator rotates the speed encoder, the front panel displays QDC counts in the range of 0 - 4095.

Test 87 - Tape in Path Sensor Check

(interactive test, tape must be unloaded)

The front panel displays * whenever the optical sensor beam is blocked.

Test 88 - Door Sensors Check

(interactive test)

The front panel displays `DOOR` whenever the door or the top cover is open. The (UNLOAD) key allows the door to be opened during this test. When the (UNLOAD) key is pressed, if the door is not detected open within one half second, then `CHECK` is displayed in the front panel.

Test 89 - Reel Encoders/Write Enable Ring Sensor Check

(interactive test) **(requires scratch tape) (tape must be unloaded)**

The tester loads a write-enabled scratch tape and spins it with his hand. The front panel displays * each time a reel encoder pulse is seen. The front panel illuminates the `WRT EN` annunciator when the write enable encoder is seen. The `WRT EN` annunciator remains lit until cleared.

Test 90 - TDU Functionality Check

(interactive test)

The TDU is engaged. After one-half second it is retracted.

Test 91 - Hub Lock Check

(interactive test) This check causes the hub to lock.

Test 92 - Hub Unlock Check

(interactive test)

This check causes the hub to unlock.

Test 93 - Load Fan Check

(interactive test)

The load fan is switched on for thirty seconds.

Test 94 - EOT/BOT Sensor Check

(interactive test)

The front panel displays `BOT` when a BOT sticker is detected. The front panel displays `EOT` when an EOT sticker is detected. This test should be performed with a tape threaded through the tape path (not tensioned). The tester can then manually turn the tape reels to move the BOT/EOT sticker past the sensors.

Test 95 - Servo Performance

(scratch tape required)

A complete check of the servo system is performed. The test performs worst case repositions, forward and reverse speed checks, high speed rewinds, etc. The buffer arm is tested for displacement, the velocity is checked for specifications, and the servo ramp rate is checked.

Test 96 - Servo Reposition Exerciser

(param A - forward time in seconds) (param B - reverse time in seconds) (scratch tape required)

The drive will continuously reposition to EOT then rewind, if param A is greater than or equal to param B. Otherwise, the drive repositions until BOT.

Test 97 - Servo Close Loops

(scratch tape required)

The ability to close the servo loops is tested.

Test 98 - Read Channel Gain Profile Display

(param A - Density)

This test displays the read channel gain profile for the selected density. The display will show TX YYY where X is the track number (1..9 and A) and YYY is the gain required for that track. The (NEXT) (PREV) keys can be used to view all the tracks. Track A is the average of all 9 tracks. The (ENTER) key is used to terminate the gain display. The gain profiles are generated by test #99 and typically saved in non-volatile memory.

Test 99 - Read Channel Calibration

(param A - density, param B - cntl) (write enabled tape required)

This test is used to calibrate the read channel gain profile. A tape which is typical of those used in the unit should be used for the calibration. This test will write a calibration pattern on the tape and then read the pattern to calibrate the drive. When the test is complete it will display the gain (see test #98). Dual density drives should be calibrated in both densities. If parameter B is set as "SAVE" then the calculated gain profile will be saved in non-volatile RAM. If parameter B is set as "TEMP" then the calculated gain profile will only be displayed after this test is complete.

Test 100 - Erase Tape

(param A - prewrite control) (scratch tape required)

This test verifies an erase from the current tape position to the end of tape marker. The tape is rewound upon encountering EOT.

Param A	Prewrite Control
0	Erase only
1	Write tape at GCR data rate first (PE for 7979)
2	Write tape at PE data rate first
3	Write tape at NRZI data rate first

Test 101 - Write Electronics Exerciser

(param A - density) (scratch tape required)

This exerciser writes an all ones pattern in the specified density from the current tape position to the end of tape marker. The tape is rewound when EOT is encountered.

Test 102 - Read Electronics Exerciser

(param A - density) (scratch tape required)

This exerciser runs from the current tape position to the end of tape marker with the read electronics switched on and setup in the specified density. The tape is rewound when EOT is encountered.

Test 103 - Read Reverse Exerciser

(param A -density) (scratch tape required)

This exerciser positions the tape at EOT then runs in the reverse direction to the beginning of tape marker with the read electronics switched on and setup in the specified density.

Test 104 - Head Crosstalk Exerciser

(param A - density) (scratch tape required)

This exerciser rewinds the tape, then runs to the EOT marker with the erase head on in order to prepare the tape for crosstalk. It then runs in the reverse direction to the beginning of tape marker with the read and write electronics on and setup in the specified density.

Test 105 - NRZI Read Skew Calibration

(param A - control) (master head alignment tape required) (test valid for option 800 drives only)

This test is used to calibrate the NRZI read de-skewing hardware. A master head alignment (skew) tape is required for this test. The test will make a forward pass from BOT to EOT during which 2000 skew measurements will be taken and then will make a reverse pass from EOT to BOT during which an additional 2000 measurements in the reverse direction are taken. If the required number of samples in either direction is not achieved in one pass the tape will be repositioned at the other end and sampling will continue. After the read passes are completed the skew correction values are calculated and displayed (see test #107). If parameter A is set as "SAVE", the calculated read skew correction values will be saved in non-volatile RAM. If parameter A is set as "TEMP", then the resulting values will be used by the hardware until either this test is executed again or the tape drive is power cycled.

Test 106 - NRZI Write Skew Calibration

(param A - control) (write enabled tape required) (test valid for option 800 drives only)

This test is used to calibrate the NRZI write de-skewing hardware. A tape typical of those used in the unit should be used for this calibration. TEST 105 "NRZI READ SKEW CALIBRATION" MUST BE EXECUTED PRIOR TO THE EXECUTION OF THIS TEST AND THE DRIVE MUST NOT BE POWER CYCLED BETWEEN THE EXECUTION OF TEST 105 AND THIS TEST. This test will write a calibration pattern on the scratch tape from BOT to EOT. The pattern will be read, the write skew correction values will be calculated and the results will be displayed (see test #107).

IF parameter A is set as "SAVE" the calculated read skew correction values will be saved in non-volatile RAM. IF parameter A is set as "TEMP" then the resulting values will be used by the hardware until either this test is executed again or the tape drive is power cycled.

Test 107 - NRZI Skew Calibration Value Display

(param A - value set)

This test displays the skew correction values currently in use for each track for the selected value set.

For read correction values, the display will show `XRTY ZZ` where X is "F" (forward) or "R" (reverse), Y is the track number (1..9) and ZZ is the correction value. Each value represents the amount of correction for the selected track and direction in increments of 78 micro-inches.

For write correction values, the display will show `FWTY ZZ` where Y is the track number (1..9) and ZZ is the correction value. Each value represents the amount of correction for the selected track in increments of 19.5 micro-inches.

The (NEXT) (PREV) keys can be used to view each track's correction value and the enter key is used to terminate the value display.

Param A	Value Set
0	Read correction values
1	Write correction values

Test 108 - Current Gain Profile Display

(param A - display select)

This test will display the gain profile for the currently loaded tape. The gain profile is read whenever a tape is identified (following a load or a rewind) or a density ID is written. select 0 will display the load gain profile for the current tape. Display select 1 will display the load gain profile for the current tape relative to the non-volatile profile. Display select 2 will the current profile used for reading and writing the tape. It is the non-volatile profile normalized to match the average gain current tape. Gains are displayed as described in Test #98. For PE tapes, display select 0 and 1 will show track 4 only (the PE ID track).

```
...
190 |                  GAIN PROFILE EXAMPLE
    |
188 | N-\
    |    \         /-N-\                    /-N-\
186 |     \N----N-/     \         /-N----N-/     \-N
    |                    \N----N-/
184 | C-\                 L
    | L  \ L       /-C-\            L       /-C-\
182 |     \C----C-/     \      L  /-C----C-/  L  \CL
    |           L    L   \C----C-/       L
180 |_ _  _ _  _ _  _ _  _ _
...   1    2    3    4    5    6    7    8    9    A
                   track

           N = NVRAM gain profile (from test #99)
           L = Load gain profile (when tape was loaded)
           C = Current R/W gain profile
```

The non-volatile gain profile is normalized such that its average N[A] is the same as the average of the load gain L[A].

Test 109 - NRZI Dynamic Skew

(write enabled tape required) (test valid for option 800 drives only)

This test measures the dynamic skew present in the tape system (ie tape path + current tape). TEST 106 MUST BE EXECUTED PRIOR TO THE EXECUTION OF THIS TEST. The test will alternately write and then read a test pattern with tracks 1 and 9 offset by a known amount of static skew. After the measurements are complete the result is calculated and displayed. The display will show "DSW xxx" where xxx represents the percentage of the measurements that fell within +- 39 micro inches of the expected offset of tracks 1 and 9. A higher value corresponds to less dynamic skew. A value >= 64 indicates the the dynamic skew is within acceptable limits.

Test 110 - Tape Pack Conditioner

(any tape)

The tape is positioned at EOT then rewound at the archive rewind speed.

Buffer Controller Tests (120 - 129)

Test 120 - Buffer Register

Write to and read values from all of the buffer registers to verify their data acceptance and retention.

Test 121 - Buffer Function

Perform push and pop operations from the buffer controller, verifying counter and address operation, parity circuitry, and prefetch latching.

Test 122 - Buffer RAM

Buffer RAM is tested for data acceptance and retention. The test is destructive to data in the data buffer.

Test 128 - Dump NVRAM to Tape

(scratch tape required)

The non-volatile RAM of the data buffer is dumped and written onto the tape as the first record, and with the appropriate header. This test should be run prior to replacing the battery. Note that this test will fail if a new blank tape is installed. Run Test 150 before Test 128 on a new tape.

Test 129 - Load NVRAM from Tape

(pre-written dump tape required)

The non-volatile RAM of the data buffer is loaded from a tape written using Test 128. This test is used to reload non-volatile RAM information following the changing of the battery or the Data Buffer PCA. After this test is run the drive must be powercycled for the interface and drive controller to receive the new non-volatile RAM values.

Data Compression Tests (130 - 139)

Test 130 - Data Compression Register (XC/SX ONLY)

Setup and verify data compression hardware modes and status registers.

Test 131 - Data Compression Functionality (XC/SX ONLY)

(param A=subtest)

Param A	Definition
0	Runs subtests 1 through 3
1	Pass through mode test
2	Normal/observation mode test
3	Normal/output disable mode test

Test 132 - Dictionary RAM (XC/SX ONLY)

Generates and loops data thru the data compression hardware to provide a high level of dictionary RAM coverage.

Test 133-Data Compression Extended Functionality (XC/SX ONLY)

(param A - ptrn)

Param A	Pattern
0	All zeros
1	All ones
2	Alternating all zeros, all ones
3	Rotating data bytes (0 to 255)
4	Pseudo random data
5	All data patterns (0 through 4)

HPIB Interface Controller Tests (140 - 149)

Test 140 - HPIB Controller

Checks out operations of the HPIB controller chip.

Tests 141 through 145 - Reserved Tests

These tests will always pass.

SCSI Interface Controller Tests (140 - 149)

Test 140 - SCSI Interface Controller Chip

Checks out operations of the SCSI interface controller chip.

Test 141 - Onboard Hardware Tests

Checks out additional onboard functions.

Tests 142 through 144 - Reserved Tests

These tests will always pass.

Test 145 - SCSI Connector Loopback

This test performs a loopback through SCSI connectors checking proper operation of the SCSI drivers, receivers and cables. This test requires an external loopback hood with terminator power.

Pertec-Compatible Interface Controller Tests (140 - 149)

Tests 140 through 145 - Reserved Tests

These tests will always pass.

Drive Command Execution (150 - 199)

The Drive Command Execution tests many of the read/write and tape handling commands, either individually from the front panel or as part of a sequence. Errors which occur while executing these commands use the runtime error set. No isolation or suspected FRUs are indicated in the error message.

Note

All of these commands with the exception of host to buffer commands require that a scratch tape be loaded. Tests 150-167 are run by the drive controller and will not perform retries.

Test 150 - Write Density ID

(param A density: 800, 1600, 625) (tape must be at BOT)

Test 151 - Write Test Record

(param A test record size)

A single record is generated within the drive controller and written to tape.

Param A	Test Record Size in Bytes
0	1
1	256
2	512
3	768
4	1024
5	1280
6	1536
7	1792
8	2048
9	2304
10	2560
11	2816
12	3072
13	3328
14	3584
15	3840

Test 152 - Write Tape Mark

Test 153 - Write Gap

(param A gap length)

Param A	Gap Length
0	2.0 inch write gap
1	4.0 inch write gap
2	8.0 inch write gap
3	12.0 inch write gap
4	16.0 inch write gap
5	Erase to EOT

Test 160 - Verify Record

(param A runaway control)

A single record is read from the tape verifying the data but without the results being placed in the data buffer. The runaway control parameter sets the maximum amount of blank tape the drive will cover while looking for the record. 0 = 25 feet, 1 = 12 inches.

Test 161 - Forward Space Block

Single blocks are spaced over without verifying any data in the blocks.

Test 162 - Backspace Block

Single blocks are spaced over without verifying any data in the blocks.

Test 163 - Forward Space File

Blocks are spaced over until a file mark in encountered.

Test 164 - Backspace File

Blocks are spaced over until a file mark in encountered.

Test 165 - Load Tape

Test 166 - Rewind

Test 167 - Unload Tape

(param A door control)

Param A	Door Control
0	Remain closed
1	Open door

Note Test 170-177 are run by the buffer controller and will perform retries.

Test 170 - Write Tape Mark to Buffer

A tape mark entry is generated in the buffer without writing it to tape.

Test 171 - Create Record in Buffer

(param A pattern)\(param B record size)

A record is created in the buffer without writing it to tape. The pattern parameter indicates the type of data to be generated.

Param A	Pattern
0	All zeros
1	All ones
2	Alternating all zeros, all ones
3	Rotating data bytes (0 .. 255)
4	Pseudo random data
5	Use existing data in buffer RAM
6	Rotating data with parity error on the last byte

Param B	Record Size in Bytes
0	1
1	256
2	1K
3	4K
4	16K
5	32K
6	64K
7	128K
8	256K

Test 172 - Write Buffer to Tape

(param A - retain data / next write control)

Write the contents of the next entry in the queue to tape. The following parameters affect the write.

remove	Remove record from buffer following the write Note that if the test is looped more times than there are buffer entries, the test will fail with an empty buffer.
retain	Retain record in buffer following the write
stream	Attempt to stream by starting to write the next record in the buffer. If no write is received, the startup is aborted and the tape repositioned.
single	Do not startup the next write. Streaming will not occur.
err normal	Fail on all errors.
err bypass	Fail on all errors except write errors. write errors will be logged in the error and error rate logs and can can be displayed using INFO.

Param A.

0 - remove / stream / err normal
1 - retain / stream / err normal
2 - remove / single / err normal
3 - retain / single / err normal
4 - remove / stream / err bypass
5 - retain / stream / err bypass
6 - remove / single / err bypass
7 - retain / single / err bypass

Test 173 - Read from Tape to Buffer

(param A - retain data / readahead control)

A record is read from the tape into the data buffer. The following parameters affect the read.

remove	Remove record from buffer following the read
retain	Retain record in buffer following the write Note that if the test is looped more times than there is room left in the buffer, the test will fail with a full buffer.
stream	Attempt to stream by starting to read the next record from the tape. If no read command is received, the startup is aborted and the tape repositioned.
single	Do not startup the next read. Streaming will not occur.
err normal	Fail on all errors.
err bypass	Fail on all errors except read errors. Read errors will be logged in the error log and error rate logs and can be displayed using INFO.

Param A.

0 - remove / stream / err normal
1 - retain / stream / err normal
2 - remove / single / err normal
3 - retain / single / err normal
4 - remove / stream / err bypass
5 - retain / stream / err bypass
6 - remove / single / err bypass
7 - retain / single / err bypass

Test 174 - Clear Data Buffer

All entries in the data buffer are removed.

Test 175 - Initialize Cumulative Log

The PE and GCR cumulative logs are cleared.

Note Tests 176/177

These tests are not available on units with a FRU 4 Buffer Controller (firmware below 6.00).

Test 176 - Buffer Write Tape Mark

A tape mark is written to the tape, with retries performed if necessary. The contents of the buffer are not affected. This test will not stream if looped.

Test 177 - Buffer Write Density ID

(param A density - 800, 1600, 6250) (tape must be at BOT)

The selected density ID is written to the tape, with retries performed if necessary. The contents of the buffer are not affected.

HPIB Host-Only Tests (200 - 255)

Test 200 - Hardware ID

This test is used to identify the hardware assemblies and options which may vary within the HPIB 1/2-inch Tape Drive products. This test is only available with firmware revisions of 3.50/6.00 or later. If this test is available, the error returned is zero and the FRU 1 field (byte 3) contains a hardware ID code as follows:

ID Code	Product #	Drive FRU	Buffer FRU	R/W FRU
0	7979A/S	'79-66503	66504	66521
1	7980A/S	'80-66503	66504	66521
2	7979A/S	'79-66503	66514	66521
3	7980A/S	'80-66503	66514	66521
4	7979A/S W/NRZI	'79-66503	66514	66531
5	7980A/S W/NRZI	'80-66503	66514	66531
6	7980XC/SX	'80-66503	66524	66521
7	7980XC/SX W/NRZI	'80-66503	66524	66531

Test 250 - Clear SelfTest Failure

This test, when run with test parameter 1 = 1, clears the poweron selftest failure status within the HPIB interface. This test is available with firmware 3.85/6.50 or later.

Test 252 - Go Offline

This test places the drive offline if it is currently online. This test is available with firmware 3.85/6.50 or later.

Test 253 - Go Online

This test places the drive online if it is currently offline. This test is available with firmware 3.85/6.50 or later.

Test 254 - Read Configuration

This test provides access to individual Configurations within the drive. Test parameter 1 must contain the Configuration parameter to access (40 .. 96). If the test is successful the error code returned will be zero, and the current value of the Configuration is returned in the FRU 1 field (byte 3). This test is available with firmware 3.85/6.00 or later.

Test 255 - Set Configuration

This test provides access to individual Configurations within the drive. Test parameter 1 must contain the Configuration parameter to access (40 .. 96). Test parameter 2 must contain the actual value to be set. If the test is successful the error code returned will be zero. This test is available with firmware 3.85/6.00 or later.

8.3 Error Messages

This section contains the following information:

- Interpretting the drive error message format
- Drive error codes and probable causes
  - Runtime/Operational Error Codes
  - Kernal Test Error Codes
  - Multiprocessor Error Codes
- Host (HPIB) Error Codes

Drive Error Message Format

For errors that occur during the "Poweron" sequence, "FAIL 0" will be displayed. To access the error information, press the ENTER key. All available information will be displayed. All of the latest errors (up to 30) can be accessed through "INFO 0". Host-based diagnostics can be used to access this information. Refer to your Pertec-Compatible or SCSI Interface Specifications for additional information.

All error messages are of the same format. All fields within the error message may not be known or applicable. An unknown field is cleared to zero. When no error is detected (test PASSed), the diagnostic result is "all zeros."

Table 8-4. Drive Error Message Format

Byte 1				Byte 2	Byte 3	Byte 4	Byte 5
P	T	U	Error Set	Error Code	FRU 1	FRU 2	Test No.
7	6	5 4	3 2 1 0				

(P) Poweron Error — This bit is set when an error occurs during poweron selftest.

(T) Time Resync — This bit indicates that the time stamp saved with the error log has no relation to that of the previous entry. It is only set by the logging routine within the data buffer as an error is logged.

(U) Unused — These two bits are not used here.

Complete Error — The complete error message which is displayed on the front panel consists of the error set combined with the error code.

Error Set — Various sets of error codes exist. The definition of the error is dependent upon which set it is taken from, as follows:

0 Runtime errors

3 Drive Controller diagnostic errors

4 Buffer Controller diagnostic errors

6 Interface Controller diagnostic errors

C Multiprocessor errors (loopback and DPR)

F Operational status (for internal use, not logged)

Error Code	Error codes for error sets 0-C are defined after this subsection.
FRU 1 and 2	Up to two FRUs may be identified by the drive as being at fault. Two isolated FRUs may be specified if the fault involves the interaction of the two FRUs. If only one FRU is being identified, the remaining FRU should be set to zero. Both FRUs are set to zero if an error is merely detected, or if an operational status message is being sent.
Test Number	The individual test number (not sequence number) which failed is included.

Error Codes and Probable Causes

These tables list error codes, probability (P%), and most probable cause for errors seen on the tape drive. A possible reason for the error is given in the Comments column.

Error codes are grouped into three categories. Each group begins with a specific number.

0xx - Runtime/Operational Error Codes

3xx, 4xx, Exx, and 6xx - Kernal Test Error Codes

Cxx - Multiprocessor Error Codes

0xx Runtime/Operational Status Codes

Oxx Runtime/Operational error codes include the following types:

- General operation errors
- Write errors
- Servo errors
- NRZI skew errors
- Buffer errors
- Interface errors
  - HPIB
  - SCSI
  - Pertec-compatible

General Operation Errors.

Table 8-5. General Operation Errors

Error Code	P%	Cause	Comments
001	90%	Tape	No tape is loaded.
	9%	Tape sensor PCA	
002	90%	Operator	Drive not ONLINE.
	9%	Control Panel	
004	90%	Tape	Tape is write protected.
	9%	Tape Sensor PCA	
005	90%	Operator	A loaded tape prevents
	9%	Tape Sensor PCA	access of this Diagnostic.
006	70%	Operator	Front Door or Top Cover
	25%	Microswitch	is open.
	4%	Tape Sensor PCA	
00A	70%	Tape	Tape NOT initialized.
	15%	Read/Write Card	
	10%	Head Assembly	
00B	50%	Operator	Ensure Tape is at BOT.
	35%	Read/Write Card	
	10%	Head Assembly	
	4%	Tape Sensor PCA	
00D	95%	BOT/EOT Sensor	Backspace at BOT is requested.
	4%	Code	This is NOT permitted.
00F	95%	Tape	Tape ten feet past EOT, cannot
	4%	Code	Write to Tape.

Table 8-5. General Operation Errors (continued)

Error Code	P%	Cause	Comments
010	55% 20% 20% 4%	Interface Controller Board Buffer Board Code	Invalid Command received from the Host.
011	55% 20% 20% 4%	Interface Controller Board Buffer Board Code	Invalid parameter received from the Host.
012	95% 4%	Controller Board Code	Invalid test or info number received from the host.
013	95% 4%	Controller Board Code	Test not remotely accessible.
014	90% 5% 4%	Operator Controller Board Buffer Board	Test aborted by Reset.
015	75% 20% 4%	Operator Controller Board Code	Test 38 was run with more steps than are permitted.
016	75% 20% 4%	Operator Controller Board Code	The system has requested a density which is not available.
017	75% 20% 4%	Operator Controller Board Code	An illegal processor was selected for processor test.
018	60% 30% 9%	Controller Board Buffer Board Code	The write record length exceeded the maximum record length supported.

Table 8-5. General Operation Errors (continued)

Error Code	P%	Cause	Comments
01C	65%	Buffer Board	Buffer is empty, cannot retrieve a record.
	25%	Controller Board	
	9%	Code	
01D	65%	Buffer Board	Buffer is full, cannot accept any additional records.
	25%	Controller Board	
	9%	Code	
01E	70%	Tape	Test 129 was run with an invalid Configuration tape.
01F	24%	Controller Board	
	5%	Buffer Board	

Read Errors.

Table 8-6. Read Errors

Error Code	P%	Cause	Comments
020	60%	Buffer Board	Buffer overrun error
	39%	Read/Write Board	
021	60%	Tape	Gap before EOD error
022	25%	Read/Write Board	3 or more tracks in error
023	14%	Head assembly	2 tracks in error
024			1 track in error
025			CRC error
026			ACRC error
027			Residual error
028	60%	Tape	Syndrome detected 1 track in error
029	39%	Read/Write Board	Formatter CRC error
02A	99%	Read/Write Board	Unknown RF Error
02B	60%	Tape	Block timeout error
02C	25%	Read/Write Board	Block detect error
02D	14%	Head Assembly	End block error
02E			Bad gap after ID error
02F			Gap check error
030			Short post-gap error
031			
032			False ID block error
033			Bad tape mark error

Table 8-6. Read Errors (continued)

Error Code	P%	Cause	Comments
039	99%	Read/Write Board	NRZI read tape mark read error.
03A 03B 03C	50% 35% 14%	Read/Write Board Head Assembly Tape	Tracks with gain too low (03A) too high (03B) or too low and too high (03C) during read channel calibration.
03F	75% 20% 4%	Operator Read/Write Board Head Assembly	Diagnostic run to read data from tape; NO data found.

Write Errors.

Table 8-7. Write Errors

Error Code	P%	Cause	Comments
040	65%	Buffer Board	Buffer underrun error.
	34%	Read/Write Board	
041	60%	Tape	Gap before EOD error
	25%	Read/Write Board	
	14%	Head Assembly	
042	60%	Tape	Three or more (042), two
043	25%	Head Assembly	(043), or one (044) tracks in
044	14%	Read/Write Board	error during a write
			operation
045	60%	Tape	A CRC error occurred during
	25%	Head Assembly	a write operation.
	14%	Read/Write Board	
046	60%	Tape	A CRC error occurred during
	25%	Head Assembly	a write operation.
	14%	Read/Write Board	
047	60%	Tape	Unrecoverable Write Error
	25%	Head Assembly	
	14%	Read/Write Board	
048	60%	Tape	One track error during write
	25%	Read/Write Board	
	14%	Head Assembly	

Table 8-7. Write Errors (continued)

Error Code	P%	Cause	Comments
049	60%	Tape	Formatter CRC error.
	25%	Read/Write Board	
	14%	Head Assembly	
04A	99%	Read/Write Board	Unrecoverable Write Error
04B	55%	Tape	Block timeout error.
	30%	Read/Write Board	
	10%	Head Assembly	
	4%	Controller Board	
04C	60%	Tape	Block detect error.
	22%	Read/Write Board	
	13%	Head Assembly	
	4%	Controller Board	
04D	60%	Tape	End block error.
	23%	Read/Write Board	
	13%	Head Assembly	
	4%	Controller Board	
04E	60%	Tape	Bad gap after ID.
	25%	Read/Write Board	
	14%	Head Assembly	
04F	60%	Tape	Gap check error.
	25%	Read/Write Board	
	14%	Head Assembly	
050	60%	Tape	Erase verify error.
	25%	Read/Write Board	
	14%	Head Assembly	
051	60%	Tape	PE ID error.
052	25%	Read/Write Board	
	14%	Head Assembly	

Table 8-7. Write Errors (continued)

Error Code	P%	Cause	Comments
053 054	60% 25% 14%	Tape Read/Write Board Head Assembly	GCR ID error.
055 056 057 058	60% 25% 14%	Tape Read/Write Board Head Assembly	GCR read error.
059 05A	60% 25% 14%	Tape Read/Write Board Head Assembly	Bad tape mark error.
05B	60% 25% 14%	Tape Read/Write Board Head Assembly	Bad tape gap error. Improper head cleaning or poorly maintained media is the most common cause.
05C	70% 25%	Buffer Board Read/Write Board	Buffer parity error.
05D	50% 30% 15% 4%	Tape Read/Write Board Head Assembly Controller Board	No Data detect error.
05E	70% 20% 9%	Tape Read/Write Board Head Assembly	No tape mark detected.
05F	70% 20% 9%	Tape Read/Write Board Head Assembly	No ID detect error.

Servo Errors.

Table 8-8. Servo Errors

Error Code	P%	Cause	Comments
060	30%	Speed Encoder	Tension Shutdown.
	25%	Motor-Power Board	
	10%	Tension Arm	
	5%	Motor Cont. Cable	
	5%	Supply Motor	
	4%	Tape	Ensure tape has EOT sticker.
061	70%	Speed Encoder	Tape speed error.
062	20%	Controller Board	
	5%	Mother Board	
063	99%	Speed Encoder	Servo unresponsive.
06E	35%	Operator	No reel found.
	25%	Tape Sensor Board	
	15%	Supply Hub	
	15%	Controller Board	
	4%	Mother Board	

Table 8-8. Servo Errors (continued)

Error Code	P%	Cause	Comments
06F	70%	Hub Lock Solenoid	Hub lock error.
	20%	Controller Board	
	5%	Mother Board	
070	40%	Operator	Reel not seated properly.
	25%	Tape Sensor Board	Ensure tape reel is not
	15%	Supply Hub	distorted.
	10%	Tape	
	5%	Controller Board	
	4%	Mother Board	
071	60%	Operator	Reel inverted.
	20%	Tape Sensor Board	
	10%	Supply Hub	
	5%	Tape	
	2%	Controller Board	
	2%	Mother Board	
072	55%	Tape	Tape stuck to reel.
	45%	Tape Sensor Board	
073	55%	Operator	Tape stuck in path.
	18%	Tape Sensor Board	
	15%	Tape	
	7%	Supply Motor	
	3%	Supply Hub	
	2%	Controller Board	
074	70%	Tension Arm	Tape tensioning error.
	20%	Controller Board	
	5%	Mother Board	

Table 8-8. Servo Errors (continued)

Error Code	P%	Cause	Comments
076	70%	Operator	Door open error.
	25%	Microswitch	
	4%	Tape Sensor Board	
077	60%	Tape	Failure to re-identify tape on rewind.
	30%	Read/Write Board	
	9%	Head Assembly	
078	50%	Tape	No BOT detected. Has BOT sticker.
	45%	BOT/EOT Sensor	
	4%	Controller Board	
07A	80%	Host	Host reset abort of tape operation.
	14%	Interface	
	5%	Controller Board	
07D	65%	Tape	Tape positioning error.
07E	25%	Speed Encoder	
07F	9%	Controller Board	
080	65%	Tape Sensor Board	Reel encoder failure.
	20%	Controller Board	
	10%	Supply Hub	
	4%	Mother Board	
083	70%	Tape	Unable to thread tape. Check tape leader.
	20%	Tape Sensor Board	
	9%	Supply Motor	
084	60%	Motor Power Board	Open loop motor error
	25%	Supply Motor	
	14%	Hub Lock Solenoid	
085	65%	Read/Write Board	Gap timer error
	30%	Controller Board	
	4%	Mother Board	

NRZI Skew Errors. There have not been enough reported errors to compute the probability of occurrence (P%). Therefore, the error codes are listed with the meaning listed in the comments column.

Table 8-9. NRZI Skew Errors

Error Code	P%	Cause	Comments
086			Invalid measurement error.
087			Read skew test not executed.
088			Skew measurement verify error.
089			Corrupt skew measurement data.
08A			Measurement limit exceeded.
08B			Excessive write skew.
08C			Excessive write correction.
08D			excessive dynamic skew.

Buffer Errors.

Table 8-10. Buffer Errors

Error Code	P%	Cause	Comments
0A0 0A1	75% 15% 9%	Buffer Board Read/Write Board Interface	Buffer Parity error
0A2	75% 24%	Buffer Board Read/Write Board	Byte count mismatch
0A4	99%	Operator	Config 55 not set to 0.
0A5	80% 19%	Interface Code	Illegal size record requested.
0A8	55% 30% 10% 4%	Tape Speed Encoder Read/Write Board Controller Board	Tape position synchronization mismatch
0BF	99%	Code	Fatal error encountered.

Interface Errors —HPIB Only. There have not been enough reported errors to compute the probability of occurrence (P%). Therefore, the error codes are listed with the meaning listed in the comments column.

Table 8-11. Interface Errors —HPIB Only

Error Code	P%	Cause	Comments
0C0			Request DSJ expected.
0C5			Data Byte expected.
0C8			Command phase error.
0CC			Cold load protocol error.
0CD			HPIB sequence protocol error.
0CE			End complete expected.
0D0			End data expected.
0D2			Improper secondary.
0D3			Misplaced data byte.
0D6			Loopback protocol error.
0D7			Selftest protocol error.
0DA			HPIB parity error.
0DB			Reset by operator.
0DC			Data parity error.
0F0			Invalid tape command.
0F1			Selftest failure.

Interface Errors — SCSI Only.

Table 8-12. Interface Errors — SCSI Only

Error Code	P%	Cause	Comments
0C0	99%	Code	This command not supported.
0C2	99%	Code	There is an illegal field in the CDB.
0C3	99%	Code	There is an illegal mode select parameter.
0C4	99%	Code	The mode length is not on a legal boundary.
0C5	99%	Code	There was a fixed bit set, drive not in fixed mode.
0C7	99%	Code	Byte compare bit not supported.
0C8	99%	Operator	A front panel reset occurred.
0C9	99%	Code	SILI bit is set in fixed mode.
0CA	99%	Code	A rewind was requested while offline.
0CC	45% 39% 15%	Interface Buffer Board Read/Write Board	A parity error was detected.
0CD	99%	Code	An invalid log was requested.
0D0	70% 25%	Interface Buffer Board	A spurious reset occurred.
0D1	99%	Interface	A spurious SCSI chip interrupt occurred.
0D2	99%	Code	Requested write length too great.
0D3	99%	Code	Verify Immediate not supported.
0D4	99%	Code	Illegal message caused abort.
0D5	99%	Code	Invalid LUN was detected.

Table 8-12. Interface Errors — SCSI Only (continued)

Error Code	P%	Cause	Comments
0D7	99%	Code	Immediate bit set when not in immediate response mode.
0D8	99%	Code	Unsupported mode page was requested.
0D9	99%	Code	Invalid mode length was requested.
0DA	99%	Code	Invalid field in the mode was detected.
0DB	99%	Code	There were non-zero reserved fields.
0DC	70% 25%	Interface	The data written to the buffer did not match the requested length.
0DE	50% 25% 10% 9% 5%	Controller Board Interface Cable Terminating Plug Code	There was a bus protocol error.
0DF	50% 25% 10% 9% 5%	Controller Board Interface Cable Terminating Plug Code	There was a failure to reselect.

Interface Errors —Pertec-Compatible Only. There have not been enough reported errors to compute the probability of occurrence (P%). Therefore, the error codes are listed with the meaning listed in the comments column.

Table 8-13. Interface Errors —Pertec-Compatible Only

Error Code	P%	Cause	Comments
0C0			I/O fault error.
0C1			Density not available.
0C2			Front panel reset.
0C3			Protocol reset error.
0C4			Host reset error.
0C5			Hard error offline.

3xx, 4xx, 6xx, and Exx Kernel Test Error Codes

This section lists the following error codes types:

- 3xx - Drive Controller Diagnostic Error Codes
- 4xx, Exx - Buffer Controller Error Codes
- 6xx - Interface Controller Error Codes

3xx Drive Controller Diagnostic Error Codes.

Table 8-14. 3xx Drive Controller Diagnostic Error Codes

Error Code	P%	Cause	Comments
301	95%	Controller Board	ROM checksum error.
	4%	Program Module Kit	
302	95%	Controller Board	RAM (or DPRAM) test error.
	4%	Buffer Board	
303	99%	Controller Board	RAM test error.
304	99%	Controller Board	Complete RAM test error.
308	99%	Controller Board	Timer error.
309	99%	Controller Board	Microprocessor test error.
346	65%	BOT/EOT Sensor	Supply reel optical sensor cable not connected.
	20%	Tape Sensor Board	
	10%	Controller Board	
	4%	Mother Board	
348	75%	Speed Encoder	Speed encoder cable not connected.
	20%	Controller Board	
	4%	Mother Board	
349	75%	BOT/EOT Sensor	BOT/EOT sensor cable not connected.
	20%	Controller Board	
	4%	Mother Board	
34A	75%	Front Panel Cable	Front panel cable not connected.
	10%	Controller Board	
	10%	Control Panel	
	4%	Mother Board	
34B	75%	Interface Cable	Interface cable not connected.
	20%	Controller Board	
	4%	Mother Board	

Table 8-14.
3xx Drive Controller Diagnostic Error Codes (continued)

Error Code	P%	Cause	Comments
34C	40%	Controller Board	Interface cable plugged into Slave connector.
	35%	Interface	
	15%	Mother Board	
	5%	Interface Cable	
	4%	Buffer Board	
34D	45%	Controller Board	Slave cable plugged into Interface connector.
	35%	Interface	
	19%	Mother board	
34E	75%	Motor Power Board	48 volt PSU failure.
	20%	Controller Board	
	4%	Mother Board	
34F	99%	Controller Board	A to D converter failure.
350	99%	Controller Board	Speed DAC failure.
351	99%	Controller Board	Feed foward circuit failure.
352	99%	Controller Board	Gain/Load DAC failure.
353	70%	Motor Power Board	Supply motor loopback failure.
	20%	Tension Arm	
	5%	Controller Board	
354	70%	Motor Power Board	Take up motor loopback failure.
	20%	Tension Arm	
	5%	Controller Board	
355	99%	Controller Board	Quadrature decoder failure.
356	99%	Controller Board	Tachometer circuit failure.
357	75%	Bezel	Door failed to open.
	20%	Controller Board	
	4%	Mother Board	
358	75%	Tension Arm	Excess tension arm motion.
	15%	Controller Board	
	9%	Mother Board	

Table 8-14.
3xx Drive Controller Diagnostic Error Codes (continued)

Error Code	P%	Cause	Comments
359	75%	Supply Motor	Servo ramps too slow.
	15%	Controller Board	
	9%	Motor Power Board	
361	75%	Speed Encoder	Tape speed error.
	15%	Controller Board	
	9%	Motor Power Board	
362	75%	Supply Motor	Tape ramping error.
	15%	Controller Board	
	9%	Motor Power Board	
364	75%	Tape Displacement Unit	TDU inoperative.
	15%	Controller Board	
	9%	Read/Write Board	
365	75%	Tape Displacement Unit	TDU is slow.
	15%	Controller Board	
	9%	Read/Write Board	
366	75%	Tape Displacement Unit	TDU is slightly slow.
	15%	Controller Board	
	9%	Read/Write Board	
372	99%	Read/Write Board	Missing or unsupported revision R/W assembly.
3FF	85%	Buffer Board	Buffer controller not responding.
	10%	Controller Board	
	4%	Mother Board	

4xx, Exx Buffer Controller Error Codes.

Table 8-15. 4xx, Exx Buffer Controller Error Codes

Error Code	P%	Cause	Comments
401	95% 4%	Buffer Board Program Module Kit	ROM checksum error.
402	95% 4%	Buffer Board Interface	RAM test error (non-destructive data).
403	99%	Buffer Board	RAM test error (non- destructive data).
404	99%	Buffer Board	Complete RAM test failure.
405	99%	Buffer Board	Error in testing controlled area of non-volatile RAM.
407	45% 30% 20% 4%	Interface Cable Interface Buffer Board Mother Board	Connectivity test failure.
409	99%	Buffer Board	Microprocessor test error.
40A	95% 4%	Buffer Board Motor Power Board	Error in checksum of controlled area of non-volatile RAM.
40E	50% 49%	Buffer Board Controller Board	DPRAM test error (test 51) in offboard DPRAM.
433	99%	Buffer Board	Parity error in Push data.
434	99%	Buffer Board	Parity error in Pop data.
435	99%	Buffer Board	Error found in pre-fetch circuitry.
436	99%	Buffer Board	Pop data mismatch in buffer function test.

Table 8-15. 4xx, Exx Buffer Controller Error Codes (continued)

Error Code	P%	Cause	Comments
437	99%	Buffer Board	Push end of data status error.
438	99%	Buffer Board	Push interrupt circuit error.
439	99%	Buffer Board	Pop end of data status error.
43A	99%	Buffer Board	Pop interrupt circuit error.
43E	99%	Buffer Board	Error in buffer dynamic RAM test.
446	99%	Buffer Board	Error in Push counter extend register of buffer USM.
447	99%	Buffer Board	Error in Push counter upper register of buffer USM.
448	99%	Buffer Board	Error in Push counter lower register of buffer USM.
449	99%	Buffer Board	Error in Push address extend register of buffer USM.
44A	99%	Buffer Board	Error in Push address upper register of buffer USM.
44B	99%	Buffer Board	Error in Push address lower register of buffer USM.
44C	99%	Buffer Board	Error in Pop counter extend register of buffer USM.
44D	99%	Buffer Board	Error in Pop counter upper register of buffer USM.
44E	99%	Buffer Board	Error in Pop counter lower register of buffer USM.
44F	99%	Buffer Board	Error in Pop address extend register of buffer USM.
450	99%	Buffer Board	Error in Pop address upper register of buffer USM.

Table 8-15. 4xx, Exx Buffer Controller Error Codes (continued)

Error Code	P%	Cause	Comments
451	99%	Buffer Board	Error in Pop address lower register of buffer USM.
481	74% 25%	Operator Buffer Board	Checksum error in non- volatile RAM load from tape.
482	74% 25%	Operator Buffer Board	Byte count mismatch in non-volatile RAM load from tape.
483	74% 25%	Operator Buffer Board	Buffer header mismatch in non-volatile RAM load from tape.
484	74% 25%	Operator Buffer Board	Attempt to load data from tape int illegal address (not RAM).
490			Hardware error in data compression circuitry.
491			Bad parity from data compression circuitry.
492			Data improperly flushed from data compression circuitry.
493			Bad parity from interface into data compression circuitry.
494			Bad parity from buffer into data compression circuitry.
495			Data compression to interface byte count mismatch.
496			Data compression to buffer byte count mismatch.

Table 8-15. 4xx, Exx Buffer Controller Error Codes (continued)

Error Code	P%	Cause	Comments
4A0			Data compression chip status byte 0 error.
4A1			Data compression chip status byte 1 error.
4A2			Data compression input byte count error.
4A3			Data compression output byte count error.
4A4			Data compression chip interrupot circuit error.
4A5			Data compression chip functional error.
4FF	50% 35% 10% 4%	Interface Cable Interface Buffer Board Mother board	Interface not responding.
Exx			Fatal internal error(xx) encountered.

6xx General Interface Controller Error Codes.

Table 8-16. 6xx Interface Controller Error Codes

Error Code	P%	Cause	Comments
601	95% 4%	Interface Program Module Kit	ROM checksum error.
602	99%	Interface	RAM test error (destructive data).
603	99%	Interface	RAM test error (non- destructive data).
604	99%	Interface	Complete RAM test error.
607	60% 39%	Buffer Board interface	Connectivity test error.
609	99%	Interface	Microprocessor test error.
66E	75% 20% 4%	Interface Interface Cable Buffer Board	Error in Write loopback with good data.
66F	75% 20% 4%	Interface Interface Cable Buffer Board	Error in Read loopback with good data.
670	75% 20% 4%	Interface Interface Cable Buffer Board	Parity error in Write loopback not detected.
671	75% 20% 4%	Interface Interface Cable Buffer Board	Parity error in Read loopback not detected.
672	75% 20% 4%	Interface Interface Cable Buffer Board	Loopback compare error.

HPIB-Specific Interface Error Codes. There have not been enough reported errors to compute the probability of occurrence (P%). Therefore, the error codes are listed with the meaning listed in the comments column.

Table 8-17. HPIB-Specific Interface Error Codes

Error Code	P%	Cause	Comments
646			HP-IB controller loopback error.
647			EOI test error.
648			Inbound FIFO jammed.

SCSI-Specific Interface Error Codes.

Table 8-18. SCSI-Specific Interface Error Codes

Error Code	P%	Cause	Comments
646	99%	Interface	SCSI controller register error.
647	99%	Interface	SCSI controller RAM error.
648	99%	Interface	SCSI controller message error.
649	99%	Interface	SCSI controller command error.
64A	99%	Interface	SCSI controller kill error.
64B	99%	Interface	SCSI controller request error.
64C	99%	Interface	SCSI controller target sequence error.
64D	99%	Interface	SCSI controller command sequence error.
64E	99%	Interface	SCSI controller status sequence error.
650	99%	Interface	Hardware clear error.
651	99%	Interface	Hardware EOD error.
652	99%	Interface	Hardware "walking ones" error.
65B	95% 4%	Interface Buffer Board	SCSI Controller request error.
660	99%	Interface	Connector loopback error in DB0 or I/O.
661	99%	Interface	Connector loopback error in DB1 or C/D.
662	99%	Interface	Connector loopback error in DB2 or MSG.

Table 8-18. SCSI-Specific Interface Error Codes (continued)

Error Code	P%	Cause	Comments
663	99%	Interface	Connector loopback error in DB3 or REQ.
664	99%	Interface	Connector loopback error in DB4 or ACK.
665	99%	Interface	Connector loopback error in DB5 or ATN.
666	99%	Interface	Connector loopback error in DB6 or SEL.
667	99%	Interface	Connector loopback error in DB7 or BSY.
668	99%	Interface	Connector loopback error in DBP or RST.

Cxx Multiprocessor Error Codes

Table 8-19. Cxx Multiprocessor Error Codes

Error Code	P%	Cause	Comments
C07	39%	Buffer Board	Connectivity test error.
	30%	Interface	
	30%	Controller Board	
C0E	39%	Buffer Board	Onboard dual-port RAM test
	30%	Interface	error.
	30%	Controller Board	
C0F	39%	Buffer Board	Offboard dual-port RAM test
	30%	Interface	error.
	30%	Controller Board	
C10	39%	Buffer Board	Subordinate detected dual-port
	30%	Interface	RAM collision test error.
	30%	Controller Board	
C11	39%	Buffer Board	Master detected dual-port
	30%	Interface	RAM collision test error.
	30%	Controller Board	
C12	39%	Buffer Board	Error in master dual-port
	30%	Interface	RAM interrupt test.
	30%	Controller Board	
C13	39%	Buffer Board	Error in subordinate DPR
	30%	Interface	interrupt test.
	30%	Controller Board	
C66	50%	Controller Board	Pop count mismatch in loopback
	45%	Buffer Board	to formatter.
	4%	Read Write Board	
C67	50%	Controller Board	Push count mismatch in loopback
	49%	Buffer Board	to formatter.
C68	50%	Controller Board	Parity error not detected
	49%	Buffer Board	in loopback to formatter.

Table 8-19. Cxx Multiprocessor Error Codes (continued)

Error Code	P%	Cause	Comments
C69	50%	Controller Board	Data mismatch in loopback to formatter (return data)
	45%	Buffer Board	
	4%	Read Write Board	
C6A	50%	Controller Board	Buffer overrun not detected.
	49%	Buffer Board	
C6B	50%	Controller Board	Buffer underrun not detected.
	45%	Buffer Board	
	4%	Read Write Board	
C6E	50%	Buffer Board	Error in write loopback with good data.
	49%	Interface	
C6F	50%	Buffer Board	Error in read loopback with good data.
	49%	Interface	
C70	50%	Buffer Board	Parity error in write loopback not detected.
	49%	Interface	
C71	50%	Buffer Board	Parity error in read loopback not detected.
	49%	Interface	
C72	50%	Buffer Board	Parity error in read loopback not expected.
	49%	Interface	
CC8	50%	Buffer Board	Loopback timeout.
	49%	Interface	

Note

If you encounter a "Cxx" that is not listed in this table check under the "4xx" and "6xx" error codes to see if the "xx" appears.

Host (HPIB) Error Codes

The following is a list of the HPIB reported error codes and their corresponding HP7979A/S/7980A/S internal (CCL) error codes which could have occurred. For descriptions of the HP-IB error codes see the description of Status Register #5. For descriptions of the CCL error codes see "7979A/S/7980A/S CCL Errors."

HBIB Error	Possbile 7979A/S/7980A/S Internal (CCL) Error Codes
	(all errors in decimal)
0	0
5	4
6	1
7	22
9	10
10	11
11	02
16	12
19	13
24	16, 17, 240
31	24
33	241
45	34, 35, 36, 66, 67
47	81, 82, 83, 84, 85, 86, 87, 88, 89, 90
48	49, 91
49	44, 50, 76
51	33, 45, 65, 77
53	37, 38, 39, 69,70,71
55	118
59	68
60	32
61	43, 47, 75
63	51
82	98
83	96, 116
88	46, 48, 78, 79
90	120
91	97
94	52, 53, 125, 126, 127
95	110, 111, 112, 113, 114, 115

HBIB Error	Possbile 7979A/S/7980A/S Internal (CCL) Error Codes
102	42, 74
104	80
105	93
123	166
125	165
129	92, 160, 161, 220
130	64
131	162
140	25, 26, 163, 164
141	128
150	168
151	169, 170, 171, 172, 173, 174, 175
152	176, 177, 178, 179, 180, 181, 182
162	192
167	197
168	198
170	200
174	204
175	205
176	206
178	208
180	210
181	211
184	214
185	215
188	218
189	219
254	All reserved CCL error codes 94,95 *** revision 3.40 and earlier firmware return these errors here. They should be mapped to HPIB error #47, and will be fixed in the future.
255	3, 5, 7, 8, 9, 14, 18, 19, 20, 21, 23, 28, 29, 30, 31, 117

7979A/S / 7980A/S CCL Errors

The following table lists the Internal CCL error code definitions of the HP 7979A/S and 7980A/S. These errors are NOT the error codes returned to the host within the 6-byte status report. The HPIB error codes are described in the description of status register #5. This table describes the CCL compared to the HP-IB codes in the previous table.

Command Reject Error Codes (1 - 31).

1 (01H) = No tape is loaded.

2 (02H) = Drive is not online.

3 (03H) = Drive is not offline.

4 (04H) = Drive is write protected.

5 (05H) = Tape loaded prevents access to test.

6 (06H) = Front door or top cover is open.

7 (07H) = Controller is currently in diagnostic/options mode.

8 (08H) = Controller is not in diagnostic mode.

9 (09H) = Drive not streaming (when streaming command was received).

10 (0AH) = Cannot read tape with unidentified or unsupported format.

11 (0BH) = Cannot write tape with unidentified or unsupported format.

12 (0CH) = Tape not positioned at BOT for write density ID command.

13 (0DH) = Tape already at BOT when backspace command was issued.

14 (0EH) = Tape past EOT.

16 (10H) = Unknown or unsupported command received.

17 (11H) = Invalid parameter for requested command.

18 (12H) = Invalid test/info number.

19 (13H) = Test not remotely accessable.

20 (14H) = Test aborted by reset.

21 (15H) = User defined sequence is full, can't add test to sequence.

22 (16H) = Requested density is not available.

23 (17H) = Invalid target id for command.

24 (18H) = Requested write record length exceeded maximum supported.

25 (19H) = Write record request did not precede write record transfer

26 (1AH) = Write record transfer did not follow write record request.

27 (1BH) = Command rejected due to poweron selftest failure.

28 (1CH) = Buffer is empty, cannot retrieve record from buffer.

29 (1DH) = Buffer is full, cannot place record in buffer.

30 (1EH) = Invalid header on non-volatile memory read.

TAPE READ ERRORS (32 - 63)

32 (20H) = Buffer overrun.

33 (21H) = Gap detected before end of data on read.

34 (22H) = Two or more tracks in error on read.

35 (23H) = Two tracks in error on read.

36 (24H) = Single track in error on read (NRZI only).

37 (25H) = CRC error on read.

38 (26H) = ACRC error on read.

39 (27H) = residual error on read.

40 (28H) = syndrome detected single track in error on read.

41 (29H) = formatter CRC error on read.

42 (2AH) = Unknown formatter error on read.

43 (2BH) = Data block timeout.

44 (2CH) = Block detect error.

45 (2DH) = End block detect error.

46 (2EH) = Bad gap after ID.

47 (2FH) = Gap check timeout.

48 (30H) = Short gap after block.

49 (31H) = Block overrun.

50 (32H) = False ID block detected.

51 (33H) = Bad tape mark read.

52 (34H) = Hitch into a block failed.

53 (35H) = Hitch into a gap failed.

58 (3AH) = Tracks with gain too low during autocal.

59 (3BH) = Tracks with gain too high during autocal.

60 (3CH) = Tracks with gain too low and too high during autocal.

Tape Write Errors (64 - 95)

64 (40H) = Buffer underrun.

65 (41H) = Gap detected before end of data on write.

66 (42H) = Two or more tracks in error on write.

67 (43H) = Two tracks in error on write.

68 (44H) = One track in error on write.

69 (45H) = CRC error on write.

70 (46H) = ACRC error on write.

71 (47H) = residual error on write.

72 (48H) = syndrome detected single track in error on write.

73 (49H) = formatter CRC error on write.

74 (4AH) = Unknown formatter error on write.

75 (4BH) = Data block timeout.

76 (4CH) = Data block detect error.

77 (4DH) = End data block detect error.

78 (4EH) = Bad gap after ID.

79 (4FH) = Gap check timeout.

80 (50H) = Erase verify error.

81 (51H) = PE density ID detect error.

82 (52H) = PE density ID verify error.

83 (53H) = GCR density ID detect error.

84 (54H) = GCR density ID verify error.

85 (55H) = GCR ARA burst detect error.

86 (56H) = GCR ARA burst verify error.

87 (57H) = GCR ARA ID detect error.

88 (58H) = GCR ARA ID verify error.

89 (59H) = tape mark detect error.

90 (5AH) = tape mark verify error.

91 (5BH) = Bad pregap on write.

92 (5CH) = Buffer data parity error during write record.

93 (5DH) = No block detected during write record verify.

94 (5EH) = No block detected during write tape mark verify.

95 (5FH) = No block detected during write ID verify.

Tape Positioning/Servo Errors (96 - 127)

96 (60H) = Tension shutdown.

97 (61H) = Tape speed out of specifications.

98 (62H) = Tape ramping error.

110 (6EH) = No reel found.

111 (6FH) = Hub lock failure.

112 (70H) = Reel will not seat.

113 (71H) = Reel inverted.

114 (72H) = Tape stuck to reel.

115 (73H) = Tape stuck in path.

116 (74H) = Unable to establish tension.

117 (75H) = Tape eject timeout.

118 (76H) = Door open abort.

120 (78H) = No BOT marker detected.

121 (79H) = Operator reset abort.

122 (7AH) = Host reset abort.

125 (7DH) = Last block not found.

126 (7EH) = Gap recapture position error.

127 (7FH) = Block recapture position error.

Drive Controller Errors (128 - 159)

128 (80H) = Reel size detector failure.

131 (83H) = Unable to thread tape into tape path.

132 (84H) = Open loop motor control error.

133 (85H) = Gap timer circuitry check failed.

Buffer Controller Errors (160 - 191)

160 (A0H) = Interface data parity error.

161 (A1H) = Drive data parity error.

162 (A2H) = Byte count mismatch on write or read.

163 (A3H) = Prior error reject.

164 (A4H) = Write stopped at EOT.

165 (A5H) = Zero byte record read, or requested.

166 (A6H) = Final report message was not valid.

167 (A7H) = Tape runaway during manual diagnostic commands.

168 (A8H) = Tape position syncronization mismatch.

169 (A9H) = Physical data record too small to deblock

170 (AAH) = Invalid pointer found during deblocking of physical record

171 (ABH) = Access table contents were invalid

172 (ACH) = Access table contents were incomplete

173 (ADH) = Improper byte count sum of access table entries

176 (B0H) = Hardware error detected in data compression (XC) circuitry

177 (B1H) = Bad parity detected from Data compression circuitry

178 (B2H) = Data compression circuitry not properly flushed of data

179 (B3H) = Bad parity detected from interface into data compresssion hardware

180 (B4H) = Bad parity detected from buffer into data compression hardware

181 (B5H) = Data compression-to-interface byte count mismatch

182 (B6H) = Data compression-to-buffer byte count mismatch

HPIB Detected Errors (192 - 255)

192 (C0H) = Request DSJ expected

196 (C4H) = Tape command secondary expected.

197 (C5H) = Data byte expected.

198 (C6H) = Missing EOI on tape command data byte, selftest number, or END command data byte.

200 (C8H) = Command phase protocol error for write record.

204 (CCH) = Cold load sequence protocol error.

205 (CDH) = HP-IB protocol sequence error.

206 (CEH) = END "COMPLETE" or "COMPLETE-IDLE" expected.

208 (D0H) = END "DATA" expected.

210 (D2H) = Unknown interface secondary command.

211 (D3H) = Misplaced data byte.

214 (D6H) = Interface loopback protocol error.

215 (D7H) = Run selftest protocol error.

218 (DAH) = HP-IB command parity error.

219 (DBH) = Reset by operator during a protocol sequence.

8.4 Information Logs

The section contains the following information:

- How to display an information log
- How to clean an information log
- Quick reference table of information logs
- Interpreting the information log displays
- Detailed description of information logs

Displaying An Information Log

Each of the variables and data structures are accessible from the host and from the front panel. A description of each is given below.

To display a particular information log, do the following.

1. Take the drive offline.
2. Press the [OPTION] key on the front panel. `TEST *` appears on the display.
3. Press the [NEXT] key until `INFO *` appears.
4. Press the [ENTER] key.
5. Using [PREV] or [NEXT], bring the information log number you desire into the display.
6. Press the [ENTER] key.
7. The information in the log appears.

   For those logs which contain multiple entries, the [NEXT] and [PREV] keys provide a mechanism to move through the entries. For those entries which have multiple displays, the drive automatically scrolls through all of the displays in the entry.

   The information displays for approximately two seconds.

   Each additional display will then be shown for approximately one second.
8. Press either the [ENTER] or [RESET] key to exit the display.

Clearing an Information Log

The following Information Logs can be cleared by setting the corresponding Configuration to CLEAR. Config-15 should be set to the current year if a new battery is installed.

Table 8-20. Clearing an Information Log

Log Number	Description	Configuration to Clear	Password Required	Password
Info 0	Error Log	Conf 0	No	
Info 1	Error Rate Log	Conf 1	No	
Info 3	Cumulative GCR Error Data	Conf 3	No	
Info 4	Cumulative PE + NRZI Error Data	Conf 4	No	
Info 10	Odometer	Conf 10	Yes	Conf 100 = 63; Conf 101 = 21
Info 13	Power Cycles	Conf 13	Yes	Conf 100 = 63; Conf 101 = 21
Info 15	Battery Date	Conf 15	No	
Info 20	Drive Statistics	Conf 20	No	
Info 21	Autoload Statistics	Conf 21	No	

See the "Setting or Changing Configurations" procedures later in this chapter.

Quick Reference Information Log Table

Table 8-21. Information Log Table

Log Number	Name	Description
Info 0	Error Log	Displays the last 30 error log entries
Info 1	Error Rate Log	Displays the last 20 error rate entries
Info 2	Current Error Rate	Displays soft error rate of the current tape
Info 3	Cumulative Error Data	Displays cumulative GCR error data
Info 4	Cumulative Error Data	Displays cumulative PE + NRZI error data
Info 5	Cumulative Error Rate	Displays the cumulative soft error rate in bytes per error
Info 10	Odometer	Displays the amount of tape used
Info 12	System Software Clock	Displays the system clock
Info 13	Power Cycles	Displays the number of times the drive power has been cycled
Info 15	Battery Date	Displays the last two digits of the year the battery was installed
Info 20	Drive Repositioning Statistics	Displays reposition error statistics
Info 21	Tape Autoload Statistics	Displays attempted and successful autoload statistics
Info 24	Interface Option Identification	Displays the interface option
Info 25	Firmware Rev Number	Displays the code revision numbers of all processors
Info 30	Tape Write Compression Rate	Displays the current tape compression rate as a percentage

Interpreting Information Log Displays

An Information Log can have many entries with each consisting of one or more displays.

A sample entry and its displays are given for each of the information logs.

Display Number	Looks Like	Example	Means ...
1[1]	"LABEL" DD HHH	E10 001	The display and its example is explained.

1 Display #1 of Entry 1

Where:

"Quotes"	Indicate display labels
H	Indicates a hexadecimal digit
D	Indicates a decimal digit
DeDD	Indicates exponential notation of 'D' times ten to the 'DD'

Detailed Information Log Descriptions

Info 0 - Error Log

Displays current log entries.

The error log maintains the last 30 errors which occurred within the drive . The initial error log display is for the most recent entry. The (PREV) and (NEXT) keys are used to view other entries in the log.

Display No.	Looks Like	Example	Means ...
1	"E"DD HHH	E10 001	Entry #10 in this log; 001 is the error code—a run-time error indicating "no tape loaded".
2	"FRU" DD	FRU 40	The detected FRU is the EOT/BOT Sensor, FRU #40. Up to three FRUs may display—most probable to least probable. See Table 8-3. This display may be omitted if no FRU information applies.
3	"T" DDD	T 41	The error occurred during the execution of the ROM Checksum Test #41. This display will appear only if the error occurred during the execution of a diagnostic test.
4	"*P" DDDDD	* 78978	A two-byte time stamp (in seconds) with "*" indicating that a poweron occurred since the last error was logged (i.e., no time correlation with previous entries) and "P" indicating that the error occurred during powerup. The "P" may be replaced by an additional digit in the time stamp. The error was logged 78978 seconds after the drive was powered on, and this is the first entry since the drive was powered on. (The clock rolls over approximately every 11.5 days.)

Error Rate Logs

Two error rate logs are maintained. A short-term and a long-term log. The short-term log, "Info 1 - Error Rate Log" contains multiple entries, one entry for each of the last 20 loads or density changes of the tape. Each log entry indicates what the density for the entry was.

"Info 2 - Current Error Rate" is based on the data being accumulated for the tape that is currently loaded. When the next tape is loaded or the density is changed, the data accumulated is entered into the "Error Rate Log" log and then zeroed.

The "Error Rate Log" is intended for use during normal drive operation. During diagnostic sequences, density changes occur often enough to make the "Error Rate Log" roll through entries too fast. In order to keep from losing history in the log, entries are not made in the error rate log during diagnostic sequences. Only a single entry is made which makes no distinction between PE or GCR. In short, the "Error Rate Log" is not intended for use during diagnostics.

"Info 5 - Cumulative Error Rate Log" is a long-term history containing a separate PE and GCR log of data and errors. It does not however maintain how recent the information is or which load of tape it occurred on. The cumulative error is useful during normal runtime and is also used during certain diagnostic tests. Before error rate or wellness sequences are run, the cumulative log may be initialized, allowing the accumulated data to be related to the test at hand. The side effect of initializing the cumulative log is that all accumulated data up until that time is lost. The cumulative log is updated at least on every load or density change, but may be updated more often. It is not associated with the "Current Error Rate" information as is the "Error Rate Log".

Info 1 - Error Rate Log

Displays current log entries.

An error rate log is maintained which contains a history of hard and soft errors for the past 20 loads of the tape. The results are displayed as two entries with the same log entry number. The initial error rate log display is the most recent entry in the log. The (PREV) and (NEXT) keys are used to move from the write to read displays and from one log entry to the next. Note that the entry number ("W"DD or "R"DD) of the initial display also indicates the number of entries in the log.

Display No.	Looks Like	Example	Means ...
Write Displays			
1	"W" DD "Density"	W17 PE	Indicates the beginning of write displays for entry 17. PE format was used for the operation. Available density formats are NRZ, PE, and GCR.
2	"WH" HH	WH 01	Hard write errors in hexadecimal (unrecovered errors). One hard write error occurred.
3	"WS" HHHH	WS 0003	Soft write errors in hexadecimal (recovered errors). Three soft write errors occurred.
4	"WD" DeDD	WD 3e06	Amount of data written in bytes. $3x10^6$ bytes of data were written.

Display No.	Looks Like	Example	Means ...
Read Displays			
1	"R" DD "Density"	R17 PE	Indicates the beginning of the read displays for entry 17. PE format was used for the operation. Available density formats are NRZ, PE, and GCR.
2	"RH" HH	RH 01	Hard read errors in hexadecimal (unrecovered errors). One hard read error occurred.
3	"RS" HHHH	RS 0003	Soft read errors in hexadecimal (recovered errors). Three soft read errors occurred.
4	"RD" DeDD	RD 3e06	Amount of data read in bytes. $3x10^6$ bytes of data were read.

Info 2 - Current Error Rate

Displays soft error rate of the current tape.

Display No.	Looks Like	Example	Means ...
1	"W" DeDD	W 2e07	Displays the write soft error rate in bytes per write soft error. Current write soft error rate is approximately 20 Mbytes of data per error.
2	"R" DeDD	R 3e06	Displays the read soft error rate in bytes per read soft error.

Info 3 and Info 4 - Cumulative Error Data

- INFO 3 - Displays cumulative GCR error data.
- INFO 4 - Displays cumulative PE + NRZI error data.

Cumulative error data logs are maintained containing all past occurrences of hard and soft errors as well as the total amount of data written and read. The (PREV) and (NEXT) keys are used to move from the write to the read displays.

Display No.	Looks Like	Example	Means ...
Write Displays			
1	"WH" HH	WH 01	Hard write errors in hexadecimal (uncorrected errors). One hard write error occurred.
2	"WS" HHHH	WS 0003	Soft write errors in hexadecimal (corrected errors). Three soft write errors occurred.
3	"WD" DeDD	WD 3e06	Amount of data written in bytes. $3x10^6$ bytes of data were written.
Read Displays			
1	"RH" HH	RH 01	Hard read errors in hexadecimal (uncorrected errors). One hard read error occurred.
2	"RS" HHHH	RS 0003	Soft read errors in hexadecimal (corrected errors). Three soft read errors occurred.
3	"RD" DeDD	RD 3e06	Amount of data read in bytes. $3x10^6$ bytes of data were read.

Info 5 - Cumulative Error Rate

Displays the cumulative soft error rate in bytes per error.

Display No.	Looks Like	Example	Means ...
1	"GCR/PE"	GCR	Indicates the following two displays are the cumulative Write and Read soft error rates for operations using GCR density. If PE is indicated, the following two displays are the cumulative Write and Read soft error rates for operations using PE + NRZI density.
2	"W" DeDD	W 3e03	Write soft error rate in bytes per write soft error. $3x10^3$ bytes of data per write soft error.
3	"R" DeDD	R 3e03	Read soft error rate in bytes per read soft error. $3x10^3$ bytes of data per read soft error.

Info 10 - Odometer

Displays the Odometer.

The odometer is a 6-byte value containing the amount of tape covered in 0.1 foot increments. It requires three displays.

Display No.	Looks Like	Example	Means ...
1	"1" DDDDD	1	No numbers after the display number indicates all zeros.
2	"2" DDDDD	2	No numbers after the display number indicates all zeros.
3	"3" DDDDD	3 1449	The total amount of tape is 144.9 feet.

The odometer is a protected configuration. The odometer must be initialized at some point from a Configuration tape or from the Front Panel (passwords required). Until it is initialized, it will display ***** indicating that it has not been initialized through Config. 10.

Info 12 - System Software Clock

Displays the system clock.

The system clock is four bytes long with a least count of (approx 1/20) sec. The system clock is initialized to zero when the drive is powered up. It is maintained by the drive controller within the drive controller Dual Port RAM (DPR).

All time stamps used within machine logs use the system software clock. Time is displayed in hours, minutes, and seconds of operation.

Display No.	Looks Like	Example	Means ...
1	DDDDD	0	0 Hours
2	DD	11	11 Minutes (maximum is 59 minutes)
3	DD	56	56 Seconds (maximum is 59 seconds)

Info 13 - Power Cycles

Displays the number of times the drive power has been cycled.

Display No.	Looks Like	Example	Means ...
1	DDDDD	2	Number of times the drive power has been cycled is 2.

The power cycle log is a protected configuration. It must be initialized at some point from a Configuration tape or from the Front Panel (passwords required). Until it is initialized, it will display ***** indicating that it is inoperative.

Info 15 - Battery Date

Displays last two digits of the year the battery was installed.

Display No.	Looks Like	Example	Means ...
1	DD	89	Last two digits of the year the battery was installed. This battery was installed in 1989.

Info 20 - Drive Repositioning Statistics

Displays drive repositioning statistics.

Display No.	Looks Like	Example	Means ...
1	"FM" DD	FM -7	Forward reposition error mean in mils.
2	"FV" DD	FV 13	Forward reposition error variance in mils squared.
3	"RM" DD	RM 0	Reverse reposition error mean in mils.
4	"RV" DD	RV 0	Reverse reposition error variance in mils squared.

Info 21 - Tape Autoload Statistics

Displays tape autoload statistics.

Display No.	Looks Like	Example	Means ...
1	"LS" DDD	LS 80	The percentage of successful loads.
2	"LR" DDD	LR 0	The percentage of successful loads requiring retries.
3	"LA" DDDDD	LA 5	The total number of loads attempted.

Info 24 - Interface Option Identification

Displays the interface option identification message.

Display No.	Looks Like	Example	Means ...
1	"Option"	HP SCSI	Displays the installed interface—SCSI, HPIB, or Pertec.

Info 25 - Firmware Rev Number

Displays code revision numbers of all processors.

The revision number of code within each of the processors is displayed. Four displays are sequenced with each display having the following format.

Display No.	Looks Like	Example	Means ...
1	DD DDD	8 640	Processor #1 ID number (DD=8), version number (D=6), revision number (DD=40)
2	DD DDD	3 388	Processor #2 ID number (DD=3), version number (D=3), revision number (DD=88)
3	DD DDD	4 388	Processor #3 ID number (DD=4), version number (D=3), revision number (DD=88)
4	DD DDD	16 391	Processor #4 ID number (DD=16), version number (D=3), revision number (DD=91)

Info 30 - Tape Write Compression Rate (XC/SX Models)

Displays the current tape compression rate as a percentage.

The tape write compression rate for the last compressed (XC format) tape written is displayed. The number displayed shows the amount of tape required for a normal GCR tape compared to the XC format tape generated.

Display No.	Looks Like	Example	Means ...
1	DDDDD	240	Shows the amount of tape required for a normal GCR tape compared to the XC/SX format tape generated. For example, 240 indicates 240% more data was stored—a 2.4 to 1 tape compression.

8.5 Configurations

This section includes the following information:

- Overview
- How to set or change Configurations
- How to clear Configurations
- How to store Configurations
- Quick reference table of Configurations
- Detailed description of each Configuration

Configurations Overview

Configuration values are stored in non-volatile RAM; a powerup copy is stored in normal RAM. Displaying a Configuration displays the powerup copy. Configurations are displayed using the front panel `Conf xx` option.

A Configuration can be changed in RAM by selecting the Configuration number and its desired value. To change a Configuration and store it in NV-RAM, Configuration 40 must be enabled.

After Revision 3.40 Firmware:

With firmware revision 3.40, individual Configurations can be locked or locked. Lock Configurations require passwords. The following sections, "Setting or Changing Configurations", explain these procedures.

Setting or Changing Configurations

Setting or changing a Configuration requires four steps:

- If the Configuration is "locked", change Configurations 100 and 101 to unlock the Configuration.
- Enable a change to the non-volatile memory by switching Configuration 40 to ON.
- Select and change the Configuration of choice.V
- Switch Configuration 40 back to OFF.

1. If the Configuration is "locked", follow the steps in "Unlocking/Locking Configurations" to unlock the desired Configuration.

   If you access a Configuration and INVALID displays, the Configuration is locked.

2. Enable a change to non-volatile memory by doing the following steps.
   a. Take the drive offline. (Press (ONLINE), if necessary.)
   b. Press (OPTION) to enter the Option Mode. TEST * appears in the display.
   c. Press (NEXT) to bring Conf * into the display.
   d. Press (ENTER) to select the Configuration set mode.
   e. Using (NEXT) or (PREV) bring Configuration number *40* into the display.
   f. Press (ENTER). The display shows the current setting for Configuration 40. This Configuration should normally be OFF.
   g. Use (NEXT) or (PREV) to bring ON into the display.
   h. Press (ENTER). Values currently in non-volatile memory may now be changed.

      The display will show SET 40 for about 1 second to Confirm that it has placed the value for ON in Configuration 40. Then, Conf * re-appears in the display.

3. Select and change the configuration by doing the following steps.
   a. Press (ENTER) to select the Configuration set mode again.

b. Use NEXT or PREV to bring the desired Configuration number into the display.

c. Press ENTER. The display shows the current value for the selected Configuration.

d. Use NEXT or PREV to bring your value choice into the display.

e. Press ENTER.

The display will show `SET xx` for about 1 second to Confirm that the selected value was set. `Conf *` re-appears in the display.

4. Disable a change to non-volatile memory by doing the following steps.

a. Press ENTER to select the Configuration set mode again.

b. Bring the Configuration number *40* into the display.

c. Press ENTER.

d. Use NEXT or PREV to bring `OFF` into the display.

e. Press ENTER. Values currently in non-volatile memory may not be changed.

The display will show `SET 40` for about 1 second to Confirm that it has placed the value for OFF in Configuration 40. Then, `Conf *` re-appears in the display.

5. Exit Configuration mode by pressing RESET.

6. Switch the drive online by pressing ONLINE.

Unlocking/Locking Configurations

As the service representative, you will be called on to change the value of a locked Configuration or change a Configuration to be permanently unlocked or locked.

To Change the Value of a Locked Configuration

1. Take the drive offline. (Press [ONLINE], if necessary.)
2. Enter the passwords into Conf 100 and Conf 101 so that access to locked Configurations is enabled.
   a. Select `Conf 100` and set it to 48. (48 is the Conf 100 password.)
   b. Select `Conf 101` and set it to 76. (76 is the Conf 101 password.)
3. Enable a change to non-volatile memory by doing the following steps.
   a. Select `Conf 40` and set it to `ON`. (Keeps the change in NVRAM.)
4. Select `Conf xx` (xx is the desired Configuration number) and set it to the desired Configuration choice.
5. Change `Conf 40` to `OFF`.
6. Exit Configuration mode by pressing [RESET].
7. Cycle the power to OFF to erase the passwords. This permanently changes the value of the locked configuration. The configuration remains locked.

To Unlock or Lock a Configuration

Follow these steps to either:

- Unlock a Configuration so the user can change it from the front panel; or
- Lock a Configuration so the user cannot change it from the front panel.

1. Take the drive offline. (Press (ONLINE), if necessary.)
2. Enter the passwords into Conf 100 and Conf 101 so that access to locked Configurations is enabled.
   a. Select `Conf 100` and set it to 48. (48 is the Conf 100 Configuration change password.)
   b. Select `Conf 101` and set it to 76. (76 is the Conf 101 Configuration change password.)
3. Enable a change to non-volatile memory by doing the following steps.
   a. Select `Conf 40` and set it to `ON`. (Keeps the change in NVRAM.)
4. Determine where the Configuration lock setting is stored by adding 100 to the Configuration number.

   For example, the lock for Configuration 82 is stored in Configuration 182. (82 + 100 = 182)
5. Select the `Confxx` determined in the previous step.
6. Switch `Confxx` to `OFF` to unlock the Configuration or to `ON` to lock the Configuration.
7. Select and change `Conf 40` to `OFF`.
8. Exit Configuration mode by pressing (RESET).
9. Cycle the power to OFF to erase the passwords.

Storing Configurations

You should keep a tape record of the Configurations you are using in the drive. This enables you to restore your Configurations after any service that requires power to be removed from the non-volatile memory.

Configurations are saved to tape by running Test 150 and then Test 128. Configurations are reloaded into the non-volatile memory by running Test 129.

Quick Reference Table of Configurations

Table 8-22. 1/2-inch Tape Drive Configurations

Description	No.	Choices	Lock Unlock	HPIB Defaults	SCSI Defaults	Pertec Defaults
Clear Info Log 0	0		Unlock			
Clear Info Log 1	1		Unlock			
Clear Info Log 3	3		Unlock			
Clear Info Log 4	4		Unlock			
Clear Info Log 10	10		Lock			
Clear Info Log 13	13		Lock			
Change Info Log 15	15		Unlock			
Clear Info Log 20	20		Unlock			
Clear Info Log 21	21		Unlock			
Enable FP change	40	Off/On	Unlock HPIB	Off	Off	Off
Auto online	41	Off/On	Unlock HPIB	Off	Off	On
Media removal	42	Off/On	Lock All	On	On	On
Operator timeout[1]	43	Off/1-99	Unlock HPIB	10	10	10
Archival rewind	44	REW/ATC	Unlock HPIB	REW	REW	REW
Operator select archive	45	Off/On	Unlock HPIB	Off	Off	Off

1 Rev 6.xx firmware only.

Table 8-22. 1/2-inch Tape Drive Configurations (continued)

Description	No.	Choices	Lock Unlock	HPIB Defaults	SCSI Defaults	Pertec Defaults
Density	46	1600 ..	Lock All	6250	6250	6250
FP density control[2]	47	OPEN..	Lock All	OPEN	OPEN	OPEN
Compression control[3]	47	XC Off..	Unlock HPIB	XC On	XC Off	XC Off
Language	48	0-99	Unlock HPIB	0	0	0
Recovered error rpt	49	Off/On	Lock All	On	On	Off
Immediate response	50	Off/On	Lock All	On	On	On
TM to disable IR	51	Off/1-99	Lock All	2	2	2
Write retry count	52	0-40	Lock All	17	17	17
1600 PE,NRZI gap size	53	0-15	Lock All	6	6	6
6250 GCR gap size	54	0-22	Lock All	4	4	0
Stop at EOT	55	Off/On	Lock All	Off	Off	Off
Write holdOff timeout[4]	56	0-20	Lock All	5	5	5
Wrt holdoff timeout[5]	56	0-99	Lock All	20	20	20
Write startup point[3]	57	1-7	Lock All	2	2	2
Write startup point[4]	57	Off/1-7	Lock All	Off	Off	Off

1 Non-XC/SX drives only.

2 XC/SX drives only.

3 FRU 4 Buffer Controller

4 FRU 14 or 24 Buffer Controller

Table 8-22. 1/2-inch Tape Drive Configurations (continued)

Description	No.	Choices	Lock Unlock	HPIB Defaults	SCSI Defaults	Pertec Defaults
Write skip start	58	0-3	Lock All	2	3	3
Write control	59	0-31	Lock All	1	1	1
Readaheads	60	Off/On	Lock All	On	On	On
TMs to terminate RA	61	Off/1-99	Lock All	2	2	2
Read retry count	62	0-99	Lock All	9	9	9
Trailing buffer	63	0-6	Lock All	0	0	0
Read startup point	64	1-7	Lock All	2	2	2
Max phys rec size[6]	65	1-32	Lock All	15	15	15
Max phys rec files[1]	66	Off/1-99	Lock All	Off	Off	Off
Max phys rec bytes[1]	67	Off/1-99	Lock All	Off	Off	Off
Expansion protect[1]	70	Off/On	Lock All	On	On	On
XC opt period[1]	73	Off/1-4	Lock All	Off	Off	Off
XC opt threshhold[1]	74	Off/1-63	Lock All	32	32	32

1 XC/SX Only

Table 8-22. 1/2-inch Tape Drive Configurations (continued)

Description	No.	Choices	Lock Unlock	HPIB Defaults	SCSI Defaults	Pertec Defaults
Gage usage	75	0 - 3	Lock All	0	0	0
No break on failure	76	Off/On	Lock All	Off	Off	Off
Activity Indicator	77	Off/1-3	Lock All	Off	Off	Off
Lock host density[1,3]	78	Off/On	Lock All	Off	Off	Off
Lock interface addr[3]	79	Off/On	Lock All	Off	Off	Off
Enable INT NV change[2]	80	Off/On	Lock All	Off	Off	Off

1 Pertec and SCSI only. Not supported by HP-IB.

2 Not available from the front panel.

3 Firmware Revs above 3.80 and 6.50 only.

Table 8-23. HPIB-Specific Configurations

Description	No.	Choices	Lock Unlock	HPIB Defaults	SCSI Defaults	Pertec Defaults
Unload after rewind	81	Off/On	Unlock	Off		
HP7978/7980 HPIB ID	82	ID	Lock	7980		
Return logs select[1]	96	0 - 4	Unlock	0		

1 Firmware revisions above 6.00 only.

Table 8-24. Pertec-Specific Configurations

Description	No.	Choices	Lock Unlock	HPIB Defaults	SCSI Defaults	Pertec Defaults
Compatibility	81	1 - 2	Unlock			1
Read reverse	82	1 - 2	Unlock			2
Fast read	83	1 - 2	Unlock			2
Hard err offline	84	1 - 2	Unlock			2
Report BOT write	85	Off/On	Unlock			Off
Write xfer rate	86	0 - 25	Unlock			9
Read xfer rate	87	0 - 25	Unlock			9
Write delay	88	0 - 3	Unlock			0
Read delay	89	0 - 2	Unlock			2
Density on NRZI	90	0 - 7	Unlock			Off
EOT at early EOT	91	Off/On	Unlock			Off
Hardware density[1]	92	Off,1-2	Unlock			Off
Special options[1]	93	0 - 1	Unlock			0

1 Firmware revisions above 6.50 only.

Table 8-25. SCSI-Specific Configurations

Description	No.	Choices	Lock Unlock	HPIB Defaults	SCSI Defaults	Pertec Defaults
Block length	81	0 - 9	Unlock		0	
Bus inactivity limit [1]	82	0 - 9	Unlock		0	
Disconnect time limit	83	0 - 9	Unlock		0	
Disconnect length	84	0 - 9	Unlock		0	
Inquiry field	85	0 - 127	Unlock		0	
Interface only reset	86	Off/On	Unlock		On	
Read EOM reported	87	Off/On	Unlock		On	
SCSI II compatible	88	Off/On	Unlock		Off	
EOT reporting mode	89	0 - 3	Unlock		0	
SCSI parity checking[2]	90	Off/On	Unlock		On	
Vendor unique density[3]	91	Off/On	Unlock		On	
Suppress illegal len.[3]	92	Off,1-2	Unlock		Off	

1 Firmware revisions above 3.78 or 6.30 only.

2 Firmware revisions above 3.80 or 6.50 only.

3 Firmware revisions above 6.50 only.

Detailed Description of Configurations

Conf 0 - 21 : Clear Information Logs

Table 8-26. Configurations 0 - 21

Conf #	Description
0	Clears Information Log 0 - Error Log.
1	Clears Information Log 1 - Error Rate Log.
3	Clears Information Log 3 - Cumulative GCR Error Data
4	Clears Information Log 4 - Cumulative PE + NRZI Error Data
10	Clears and resets Information Log 10 - Odometer (password required)
13	Clears and resets Information Log 13 - Power Cycles (password required)
15	Allows setting Information Log 15 - Battery Date
20	Clears and resets Information Log 20 - Drive Statistics
21	Clears and resets Information Log 21 - Autoload Statistics

Conf 40 - Enable Front Panel NVRAM Change

Choices: Off or On

Allows permanent changes to the non-volatile Configurations to be made from the front panel. This Configuration is NOT maintained in non-volatile RAM, and is initialized to OFF at powerup.

Temporary changes can be made to unlocked Configurations without changing Conf 40. These changes will revert to their original value when the drive is power cycled.

Conf 41 - Auto Online

Choices: Off or On

Controls whether the drive automatically goes online after a tape load.

- Off means the drive does not automatically go online after a tape load.
- On means the drive does automatically go online after a tape load.

Conf 42 - Media Removal

Choices: Off or ON

This Configuration controls the ability of the operator to remove media from the drive.

This Configuration is provided for use with the SCSI host interface, and may not be applicable to other interfaces.

Conf 43 - Operator Timeout

Choices: OFF, or 1-99 seconds.

This Configuration controls the timeout used with interactive operator selections. This configuration is only available on drives with firmware revision 6.xx or above.

Conf 44 - Archival Rewind

Choices: ATC or REW.

When set to ATC (Archival Tape Rewind), the drive performs all rewind operations at a slower archive speed which allows precise packing of the tape.

This Configuration is read each time a tape is loaded. Changing this Configuration while a tape is loaded will not change how the current tape rewinds.

Conf 45 - Operator Select Archive

Choices: OFF or ON.

When ON, the drive will prompt the operator when loading a new tape to select the archive speed (ATC) or the normal speed (REW) for rewind.

Conf 46 - Density

Choices: 800, 1600, or 6250

This Configuration is the default density for a written tape. This density will automatically be written on a tape when a record is written with the drive positioned logically at BOT. The densities are as follows.

800 - 800 cpi NRZI format will be written.

1600 - 1600 cpi PE format will be written.

6250 - 6250 cpi GCR format will be written.

Conf 47 - FP Density Control (non-XC/SX).

For XC/SX drives, see the next Conf 47 description.

Choices: OPEN, LOCK, I* OPEN, I* LOCK

This Configuration controls front panel selection of write density. This configuration mode is only available on non-XC/SX Drives.

OPEN	Either the host or the front panel can select density
LOCK	Only the front panel can select density.
I* OPEN	Flash the current density in the front panel before loading a tape to allow the operator to select between the density. If the operator timeout elapses, load the tape using the selection presently flashing. This selection can be host overridden.
I* LOCK	Same as I* OPEN but the host can not override the selection.

Conf 47 - Compression Control (XC/SX)

Choices: XC OFF, XC ON, IXC OFF, IXC ON

This Configuration controls front panel selection of data compression. This configuration is only available on XC/SX drives.

XC ON	Write only 6250 tapes in compressed format unless overridden by the host.
XC OFF	Do not write any tapes in compressed format unless overridden by the host.

IXC ON	Flash XC ON on the front panel before loading a tape to allow the operator to select between XC ON and XC OFF. If 10 seconds elapse, load the tape using the selection presently flashing. This selection can be host overridden.
IXC OFF	Same as IXC ON but flash XC OFF on the front panel. This selection can be host overridden.

Conf 48 - Language

Choices: 0 - 63.

Selects the language on the control panel and the values of some display messages.

0 - English
1 - German
2 - French
3 - Spanish

Add 4 to language - replaces `READY` message with `NO TAPE`

Add 8 to language - replaces `READY` message with `UNIT #`

Add 16 to language - replaces `READING` (during retries) with `RETRY`

Add 32 to language - distributor version of front panel (with DENSITY key)

For example:

English	=	0
No Tape	=	4
Retry	=	16
Config 48 Value	=	20

Conf 49 - Recovered Error Report

Choices: OFF, 1 or 2

When configured to "Off", recovered (soft) errors will not be reported to the host. When configured to 1, all soft errors will be reported. This includes soft errors that required retries or data records corrected on the fly during reads. When configured to 2, only soft errors requiring retries will be reported.

Conf 50 - Immediate Response Enable

Choices: OFF or ON.

This variable controls the use of immediate response on write operations by the buffer controller. It must be enabled for the drive to stream writes.

Conf 51 - Tape Marks to Disable Immediate Response

Choices: OFF, or 1 - 99.

This variable contains a tape mark limit. If consecutive tape marks are received equal to or beyond this limit, Immediate Response will be disabled for that command.

Conf 52 - Write Retry Count

Choices: 0 - 40.

This variable contains the maximum retry count used by write commands before a "hard" write error status is returned to the host.

Conf 53 - PE and NRZI Gap Size

Choices: 0 - 15.

This variable sets minimum and maximum PE and NRZI gap sizes (in inches).

PE and NRZI Gap Size Selection

	Min	Max
0	0.50	0.50
1	0.50	0.60
2	0.50	1.00
3	0.50	1.50
4	0.50	2.00
5	0.60	0.60
6	0.60	1.00
7	0.60	1.50
8	0.60	2.00
9	1.00	1.00
10	1.00	1.50
11	1.00	2.00
12	1.50	1.50
13	1.50	2.00
14	2.00	2.00
15	0.60	6.00

Conf 54 - GCR Gap Size

Choices: 0 - 22

This variable sets minimum and maximum GCR gap sizes (in inches).

GCR Gap Size Selection

	Minimum	Maximum
0	0.28	0.30
1	0.30	0.30
2	0.30	0.45
3	0.30	0.60
4	0.30	1.00
5	0.30	1.50
6	0.30	2.00
7	0.45	0.45
8	0.45	0.60
9	0.45	1.00
10	0.45	1.50
11	0.45	2.00
12	0.60	0.60
13	0.60	1.00
14	0.60	1.50
15	0.60	2.00
16	1.00	1.00
17	1.00	1.50
18	1.00	2.00
19	1.50	1.50
20	1.50	2.00
21	2.00	2.00
22	0.30	6.00

Conf 55 - Stop at EOT

Choices: OFF or ON.

This variable controls the stopping of writes at EOT. When set to `ON`, all write data within the buffer when EOT is encountered must be handled manually by the interface. When set to `OFF`, writes after EOT are controlled by the host.

Valid for firmware rev 6.xx code only.

Conf 56 - Write Holdoff Timeout

Choices:

- 0 - 20 seconds. (FRU 4 Buffer Controller)
- 0 - 99 seconds. (FRU 14, 24, or 34 Buffer Controller)

With immediate response ON, write data will be held within the buffer no longer than this timeout.

Conf 57 - Fixed Write Startup Point

Choices: OFF, 1 - 7 eights of buffer or queue size.

With immediate response ON, the tape will be started up to write data when either the buffered data or the number of queued commands reaches the startup threshold. OFF disables fixed selection allowing the drive to auto select the startup point based on the conditions encountered. The OFF option is only available on units with an FRU 14, 24, or 34 Buffer Controller.

Conf 58 - Write Skip Start

Choices: 0 - 3 retries.

This Configuration will select the number of write retries to attempt before performing a write skip (gap) operation, except in diagnostics which always uses 3 retries.

Conf 59 - Write Control

Choices: 0 - 63.

This Configuration controls write related functions. The Configuration is defined in bits as follows:

Bit 0	Performs automatic write reposition when the tape is stopped during writes (add 1 to ConfIG value)
Bit 1	Short trailing erase during writes. Normally about 18 inches are erased when the tape is stopped during writes. (Add 2 to ConfIG value)
Bit 2,3	Hard write error control at 10 feet beyond EOT marker 0,0 = Hard write after 10 feet beyond EOT marker and beyond Early EOT point X,1 = No hard write after 10 feet beyond EOT marker (adds 4 to ConfIG value) 1,0 = Hard write after 10 feet beyond EOT marker (adds 8 to ConfIG value)
Bit 4	For specific OEM use only. Should be set to zero for normal operations.
Bit 5	Select data/gap threshold level (firmware revision dependent). 0 = normal head value (revision 3.85) low amplitude head value (revision 6.5x). 1 = normal head value (revision 6.5x), low amplitude head value (revision 3.85).

Conf 60 - Readahead Enable

Choices: OFF or ON.

This variable controls the use of readaheads by the buffer controller. It must be enabled for the drive to stream reads.

Conf 61 - Tape Marks to Terminate Readaheads

Choices: OFF, or 1 - 99.

This variable contains a tape mark limit across which the drive will not readahead. This Configuration is inoperative when blocked format is used.

Conf 62 - Read Retry Count

Choices: 0 - 40.

This variable contains the maximum retry count used by read commands. NRZI retry count is two times the specified retry count.

Conf 63 - Trailing Buffer

Choices: 0 - 6.

The drive has the capability of performing electronic backspacing without moving the tape, if there is data within the buffer that can be recovered. A portion of the buffer may be reserved as a trailing buffer, guaranteeing that electronic backspacing can always be performed. This Configuration is inoperative when blocked format is used. The amount reserved is as follows:

- 0 - No trailing buffer. The entire buffer is used for readaheads
- 1 - Up to 1 record or 16K bytes reserved
- 2 - Up to 2 records or 32K bytes reserved
- 3 - Up to 3 records or 48K bytes reserved
- 4 - Up to 4 records or 64K bytes reserved
- 5 - Up to 5 records or 80K bytes reserved
- 6 - Up to 6 records or 96K bytes reserved

Conf 64 - Read Startup Point

Choices: 1 - 7 eighths of buffer or queue size.

With readaheads ON, the tape will be started up to read additional data when either the buffered data or the number of queued commands decreases to the startup threshold.

XC Option Configurations

Conf 65 - Physical Record Size

Choices: 1 - 32.

In XC format, all records and tape marks from the host are put into data records on the tape. These data records are termed "Physical" records. The nominal size of them is specified in multiples of 4K bytes as follows:

1 - 4K bytes

N - N*4K bytes

32 - 128K bytes

Conf 66 - Maximum Files per Physical Record

Choices: OFF, or 1 - 99.

This Configuration specifies the limit to the number of files or parts of files allowed within a single physical record. For example, if a value of 3 is specified, a physical record may contain up to three complete files and no more.

Conf 67 - Maximum Bytes per Physical Record

Choices: OFF, or 1 - 99.

This Configuration specifies the limit to the number of bytes from the host that is allowed within a single physical record. It is specified in multiples of 16K bytes.

Conf 68 - Reserved

Any choices or information presented are not used.

Conf 69 - Reserved

Any choices or information presented are not used.

Conf 70 - Expansion Protection

Choices: ON or OFF.

The data compression hardware can expand data that has already been compressed. If this occurs, the benefits of compressing the data are lost. The drive has the ability to watch for expansion and turn it off until it sees it compress. It is enabled or disabled by this Configuration.

Conf 71 - Reserved

Any choices or information presented are not used.

Conf 72 - Reserved

Any choices or information presented are not used.

Conf 73 - Data Compression Optimization Sample Period

Choices: OFF, or 1 - 4.

The drive has the ability to monitor the compression rate of the data as it is being received. A significant degradation in this rate indicates that the type of data has changed. If this occurs, the drive can adapt to the new data. This process of monitoring and adapting is called "optimization".

This Configuration enables or disables the optimization feature as follows:

OFF - No optimization will be performed.

1 - The compression rate will be sampled every 512 bytes.

2 - The compression rate will be sampled every 1K bytes.

3 - The compression rate will be sampled every 2K bytes.

4 - The compression rate will be sampled every 4K bytes.

Conf 74 - Data Compression Optimization Threshold

Choices: OFF or 0 - 63.

The sensitivity of the optimization feature to changes in data may be specified by a threshold. If the compression rate ever falls below this threshold, the drive will adapt to the new data. The threshold is specified as follows:

```
Where N is the value of Configuration 74,

        Threshold = (64/(64-N))
```

Front Panel Configurations

Conf 75 - Gauge Usage

Choices: 0 - 3

The gauge (tape odometer) at the bottom of the front panel may be used to indicate one of four things:

0	Relative position between BOT and EOT	(uses BOT,EOT and 10 lights)
1	Amount of data in the buffer revision 6.0 and later firmware	(64K per light uses 8 lights) (50K per light uses 10 lights)
2	Number of commands/reports in the queue revision 6.0 and later firmware	(10 per light uses 10 lights) (24 per light uses 10 lights)
3	Tape write compression ratio (XC/SX only)	(# of lights = compression ratio)

Conf 76 - No Break on Failure

Choices: OFF or ON.

Failures which occur while looping diagnostic tests or running a test sequence will not cause the test to terminate. The errors will be logged in the error log and the test continued. Each individual test, will however only run until a single error occurs.

Conf 77 - Activity Indicator

Choices: OFF, 1 - 3.

Displays an indicator in the right most digit of the front panel when there are host commands being processed during drive idle time.

1 - indicator = -

2 - indicator = --

3 - indicator = *

Conf 78 - Lock Host Density Change

Choices: OFF or ON.

This Configuration determines whether the host can change the Configured density of the drive. If this Configuration is ON the host cannot change the tape drive's Configured write density. This Configuration is supported by the PERTEC and SCSI interfaces only. This Configuration is NOT supported by HP-IB.

Conf 79 - Lock Interface Address/ID

Choices: OFF or ON.

This Configuration determines whether the interface address (or ID) can be changed from the front panel. If this Configuration is ON the interface address (or ID) is locked. When locked, the interface address (or ID) can be viewed from the front panel, but attempts to change it with the NEXT and PREV keys will display `INVALID`.

Conf 80 - Enable Interface NV Change

Choices: OFF or ON.

Not available from the front panel. This Configuration allows the interface to make changes to the non-volatile Configurations.

HPIB Interface Configurations

Conf 81 - Unload after Rewind Offline

Choices: OFF or ON

The tape will be unloaded when an offline rewind command is issued.

Conf 82 - 7978/7980 Amigo ID

Choices:

- Allows setting to 7974 or 7979 on a HP7979A/S
- Allows setting to 7978 or 7980 on a HP7980A/S
- Allows setting to 7978, 7980 or 7980XC/SX on a HP7980XC/SX

This Configuration determines the Amigo ID which the host system can read. When Configured to HP7978 (or HP7974) the device will also write density ids immediately upon receiving a Set density command. NO other compatibilities between the products are guaranteed besides those provided by their HPIB protocol specifications, and specifically, the ability to run 7978 diagnostic sequences is NOT supported. The AMIGO IDS are: HP7974=0174H, HP7978=0178H, HP7979=0179H, HP7980=0180H, HP7980XC/SX=0181H.

Conf 96 - Return Logs Select (HP7980XC/SX only)

Choices: 0 thru 4

This Configuration determines what information is returned by a read logs secondary command from the host when issued to a HP7980XC/SX. The possible values are:

0 - return all logs

1 - return error log only

2 - return error rate log only

3 - return controlled Non-volatile RAM only

4 - return drive controller logs only

The HP7979A/S and HP7980A/S only support "return all logs"

Pertec-Compatible Interface Configurations

Conf 81 - Compatibility

Choices: 1 - 2

The interface may be set to use either CIPHER or CDC PERTEC commands.

1 - CIPHER 990 compatible

2 - CDC compatible (or CIPHER 880)

Conf 82 - Read Reverse

Choices: 1 - 2

The Configuration controls the function of read reverse. This Configuration is only supported by A HP88780A REV B interface.

1 - Read reverse with forward data

2 - Read reverse with NO data transfer (space reverse)

Conf 83 - Fast Read

Choices: 1 - 2

1 - uses a shorter internal command sequence to implement the read request

2 - uses a longer internal command sequence to implement the read request

Conf 84 - Hard Error Offline

Choices: 1 - 2

A hard error during writes will cause the drive to go offline. A "BAD TAPE" or "HARD ERROR" message will flash in the display.

A hard error during writes will NOT cause the drive to go offline.

Conf 85 - Report BOT Write

Choices: OFF or ON

- A write command at BOT will not report until the write is completed to tape.
- A write command at BOT can be "Immediate Responsed" (if enabled)

Conf 86 - Write Transfer Rate

Choices: 0 thru 25

The write transfer rate controls the data transfer rate during writes. The duty cycle is defined relative to down time of the IWSTR line.

Note Transfer rates above 1.6 Mhz are for future designs. They will not work with the current implementation.

#	Rate (Mhz)	Duty Cycle
0	2.67	33%
1	2.00	50%
2	2.00	25%
3	1.60	40%
4	1.60	20%
5	1.33	50%
6	1.33	33%
7	1.14	42%
8	1.14	28%
9	1.00	50%
10	1.00	25%
11	.889	44%
12	.889	22%
13	.800	40%
14	.800	20%
15	.727	36%
16	.727	27%
17	.667	50%
18	.667	33%
19	.571	42%
20	.571	28%
21	.500	50%
22	.500	25%
23	.400	40%
24	.400	20%
25	.333	33%

Conf 87 - Read Transfer Rate

Choices: 0 - 25

The read transfer rate controls the data transfer rate during reads. The duty cycle is defined relative to down time of the IRSTR line.

(See Config 86 - Write Transfer Rate for values of transfer rates.)

Conf 88 - Write Delay

Choices: 0 - 3

This Configuration controls the write delay which is time from rising edge of IWSTR to the data strobe that latches the data into the buffer.

0 = + 40 nsec

1 = 0 nsec

2 = - 70 nsec

3 = -130 nsec

Conf 89 - Read Delay

Choices: 0 - 2

This Configuration controls the read delay which is the hold time for data after the rising edge of IRSTR.

0 = 10 nsec

1 = 130 nsec

2 = 250 nsec

Conf 90 - Density on NRZI Line

Choices: 0 - 7

0 NRZI line will only reflect if the drive is host or front panel selected to write NRZI.

1 NRZI line will reflect if the drive is host or front panel selected to write NRZI OR the current tape density is NRZI (see note below).

2 NRZI line will only reflect if the drive is host or front panel selected for GCR.

3 NRZI line will reflect if the drive is host or front panel selected to write GCR OR the current tape density is GCR (see note below).

4 NRZI line will only reflect if the drive is selected to write NRZI/GCR.

5 NRZI line will reflect if the drive is host or front panel selected to write NRZI/GCR OR the current tape density is NRZI/GCR.

6 NRZI line will only be asserted if the tape has been identified as NRZI. Density changes either host or front panel will update the NRZI line during the Ident phase of the first write at BOT.

7 NRZI line will only be asserted if the tape has been identified as GCR. Density changes either host or front panel will update the NRZI line during the Ident phase of the first write at BOT.

8 NRZI line will only be asserted if the tape has been identified as NRZI/GCR. Density changes either host or front panel will update the NRZI line during the Ident phase of the first write at BOT.

Note

If the drive is Configured to write in a density other than one which is selected to be shown on the NRZI line, then the NRZI line will be de-asserted during the Ident phase of the first write at BOT.

Conf 91 - EOT at Early EOT

Choices: OFF or ON

OFF = EOT during writes is reported after the physical EOT marker is detected

ON = EOT during writes is reported when there is about 50 feet of tape left

Conf 92 - Hardware Density Selection

Choices: OFF, 1 or 2

OFF = Hardware lines do not select density

1 = IDEN line (P2 pin 50) selects density: logic 0 = PE, 1 = GCR

2 = IHIDEN line (P1 pin 36) selects density: logic 0 = PE, 1 = GCR

Conf 93 - Special Options

Choices: 0 or 1

0 = Transfer write data as soon as hardware is ready

1 = Wait 100 uS after IDBY is asserted to transfer data (PERTEC spec.).

Conf 81 - Block Length

Choices: 0 - 9

The block length is the size that records will be written to the tape.

Configuration Value	Block length (in bytes)
0	0 (variable length blocks)
1	8
2	256
3	512
4	1K
5	4K
6	16K
7	32K
8	128K
9	256K

Conf 82 - Bus Inactivity Limit

Choices: 0 - 9

The bus inactivity limit indicates the maximum time that the target is allowed to maintain the bus busy without handshakes until it must disconnect.

For firmware revisions up to (but not including) 3.78:

Config Value	Bus Inactivity Limit (in 200 usec)
0	0FFFFH (default value)
1	0100H
2	0200H
3	0400H
4	0800H
5	1000H
6	4000H
7	6000H
8	8000H
9	0H (always disconnect as soon as possible)

For firmware revisions 3.78/6.30 and beyond:

Config Value	Limit Word (in 240 msec)	Bus Inactivity Limit (in msec)
0	0FFFFH	15000
1	00008H	2
2	00020H	8
3	00080H	30
4	00200H	125
5	00400H	250
6	00800H	500
7	01000H	1000
8	04000H	4000
9	Auto disconnect	

Conf 83 - Disconnect Time Limit

Choices: 0 - 9

The disconnect time limit indicates the minimum time that the target should remain disconnected until it attempts to reselect.

Config Value	Time Limit (in 100 usec)
0	0 (reselect immediately)
1	1
2	8
3	256
4	512
5	1K
6	4K
7	16K
8	32K
9	64K - 1

Conf 84 - Disconnect Length

Choices: 0 - 9

The disconnect length indicates the amount of data that is to be transferred between SCSI bus disconnects.

Config Value	Length (bytes)
0	0 (no limit on data transferred)
1	512
2	1K
3	2K
4	4K
5	16K
6	32K
7	64K
8	128K
9	256K

Conf 85 - Inquiry Field

Choices: 0 - 127

The inquiry field allows the user to set a seven bit user specified code in the device-type qualifier field of the inquiry data.

Conf 86 - Interface Only Reset

Choices: OFF or ON

OFF - full poweron reset when bus reset is received

ON - interface only reset when bus reset is received

Conf 87 - Read EOM Reported

Choices: OFF or ON

OFF - no EOM reported

ON - EOM reported

End of media is relative to forward and reverse motion. EOM can be either the BOT or EOT.

Conf 88 - SCSI II Compatible

Choices: OFF or ON

OFF - not SCSI II compatible

ON - SCSI II compatible

"SCSI II" is an industry standard format that is more versatile than the original SCSI format.

Conf 89 - EOT Reporting Modes

Choices: 0 - 3

0	Report EOT at EOT marker
1	Report EOT at Early EOT point
2	Set only EOM bit in sense data at EOT
3	Set EOM and volume overflow sense key at EOT

Conf 90 - SCSI Parity Checking

Choices: OFF or ON

OFF - SCSI bus parity is not checked

ON - SCSI bus parity is checked

Conf 91 - Vendor-Unique Density Reporting

Choices: OFF or ON

OFF - Vendor unique density not reported (bits 6 & 7 of density code cleared)

ON - Vendor unique density reported (in bits 6 & 7 of density code)

Conf 92 - Suppress Illegal Length

Choices: Off, 1 or 2

Off	Normal operation of SILI / ILI bits.
1	Auto suppress ILI on underlength (block size < request size) and SILI=0 (variable block mode only)
2	Do not suppress ILI on overlength (block size > request size) and SILI=1 (variable block mode only)

Configuration Passwords

Conf 100 - Config Lock Password #1

Choices: 0 - 99

48 - proper password to access Configuration locks

63 - proper password to access clearing protected Configurations

Conf 101 - Config Lock Password #2

Choices: 0 - 99

76 - proper password to access Configuration locks

21 - proper password to access clearing protected Configurations

8.6 Testing the Servo from the Front Panel

The servo selftests in the drive can be used to isolate failures to the component level. Servo failures must be tested in the open loop because once the loop is closed it is no longer possible to determine which component caused the failure. The following discussion assumes that the drive passed the poweron selftests. This means that the drive controller can perform the interactive diagnostics.

A. Autoload Failures

The following tests determine failures which affect the autoload before the tape is tensioned.

If the autoload sequence does not begin at all, check the door with Test 88.

Check the tape in path sensor with Test 87. Block the beam with a tape. Lay the tape in the casting to block the tape in path. A * should show on the front panel.

Test the reel encoder and write enable (Test 89). Load a tape on the hub. There should be three reel encoder pulses per revolution and one write enable pulse.

If these pass, then check hub lock (Test 91) and unlock (Test 92). Then check the load fan (Test 93).

B. Closed Loop Operation

First determine whether the servo loop operates in general. The most common indicator of a servo problem is loss of tension. Run the closed loop selftest (Test 97) without a tape. First notice that the motors attempt to load a tape. Move the tension arm to its operating position. The motors should come to a stop. As the arm is disturbed from this position the motors will move in opposition to the sensor. More tension will pay tape out and less tension will reel it in with the supply motor. While holding the tension arm so as to stop the motors, turn the speed sensor slowly. Both motors should rotate to oppose the sensor. This test should give a quick indication of any obvious problem with the sensors, motor drive, or motors.

Check the tension arm (Test 85). The number on the front panel should range smoothly from about 30 to 255, with the nominal arm position at about 150.

Test the shutdown limits (Test 84). The limits should occur before the arm has reached its hard stops.

Test the speed encoder (Test 86). As the encoder is spun by hand the value should change smoothly from 0 to 4095. Check for any stuck bits. If the encoder seems to malfunction, run the position counter test (Test 82). This verifies that the counter on the drive controller is operational. If Test 82 passes but Test 86 fails, then the encoder or its cable is faulty.

If the motors fail to rotate during the closed loop test, rerun the test and listen for a click of the relay. A single click indicates that the motors are being enabled, a double click indicates that the shutdown circuits are not working.

C. Motion Tests

If the problem appears to be loss of position or tension shutdown while the servo operates, check the TDU (Test 75 or 90).

If the tape runs off the BOT or EOT, check the BOT/EOT sensor assembly with Test 94. To do this test, run a piece of tape over the tape path at least one foot per second over the BOT/EOT sensor.

The top sensor is the BOT, and the bottom is EOT.

8.7 IOQ I/O Status Decode of Listlog Output

The following status values are returned by the tape driver and are found in the PCB/STAT word of a LISTLOG listing. (% = octal)

General Status (13:3)	Qualifying Status (8:5)	Overall Value
0 - Pending	1 - completion wait	%10
	3 - "Not Ready" Wait	%30
	4 - "No Write Ring" Wait	%40
1 - Successful	0 - no errors	%1
	2 - retry was necessary	%21
	3 - EOT after write	%31
2 - End-of-file	1 - A tape mark was read or P1 was non-zero and the last record read was a tape mark	%12
3 - Unusual Condition	3 - request aborted	%33
	4 - prior'ERR'abort	%43
	5 - pass'EOV'abort	%53
	6 - powerfail abort	%63
	7 - BOT and backspace requested	%73
	% 10 - tape runaway	%103
	% 11 - EOT and write requested	%113
	% 21 - device powered up	%213
	% 23 - set density and not at load point	%233
4 - Irrecoverable Error	0 - invalid request	%4
	1 - transmission error	%14
	3 - timing error	%34
	4 - SIO Failure	%44
	5 - unit failure	%54
	% 12 - system error	%124
	% 14 - channel failure	%144

Word 0, Byte 1 (Status Register #1)

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
EOF	BOT	EOT	Recov. Error	Command Reject	Write Protect	Unrec. Error	Online

BIT 7:

1 = Online

0 = Offline

This bit indicates the current status of the tape drive. It is set after the operator has loaded a tape and pressed the ONLINE Button. It is cleared when the operator presses the RESET Button, upon acceptance of the rewind-offline command, or when a tape has lost tension.

The tape drive must be online in order to accept tape commands. This condition is only checked when the command is being validated. If a tape command is issued when this bit is cleared, then the command rejected bit will be set, the command reject error class will indicate device reject, and register #5 will indicate drive not online.

Corrective action for this condition should be to prompt the user to bring the drive online and wait.

BIT 6:

1 = Unrecovered data/format error

0 = No unrecovered data/format error

This bit is set for any unrecovered recording error encountered during read or write operations. This condition can only exist after all retries have been exhausted. These errors include tape velocity or tension out of spec, formatter errors, multiple tracks in error, failure to verify a write, data format error, gap

before end of data, redundancy check error. The highest priority cause for the setting of this bit is contained in the contents of status register #5.

The multiple tracks in error condition occurs when two or more tracks were in error for a PE read or write, when two or more tracks were in error for GCR write, or when three or more tracks were in error for a GCR read.

Corrective action for this condition would be replacement of the tape, and the job run again. When this error occurs data is written or read the best the drive can.

BIT 5:

1 = Write protected

0 = Write enabled

This bit indicates that the write enable ring is missing. This bit is set when the operator has loaded a tape which has no write enable ring and is cleared when this tape is unloaded. If a write operation is attempted when this bit is set, then the command rejected bit will be set, the command rejected error class will indicate device reject, and register #5 will indicate tape is write protected.

Corrective action for this condition should be to issue a rewind offline command and request that the operator insert a write enable ring or load another tape.

BIT 4:

1 = Command rejected

0 = Command accepted

This bit is set when a command has been rejected by the drive due to a device setup error, protocol error, or selftest failure. The reason the command was rejected can be found in status register #4. Register #5 will have further error description.

Corrective action for these conditions are discussed under register #4's description.

BIT 3:

1 = Recovered error

0 = No recovered errors

This bit is used to indicate that error correction and/or retries have taken place during a tape read or write operation.

No corrective action is needed. The host may wish to log the state of this bit along with the retry count.

BIT 2:

1 = Beyond End of tape (EOT)

0 = Not beyond end of tape

This bit indicates whether the tape is currently positioned beyond the end of tape marker. This bit is set when the EOT marker is detected during the processing of a forward motion tape command. This bit is cleared when the EOT marker is detected during the processing of a reverse motion tape command. This status bit is a warning that there is 10 feet of usable recording area left and 25 feet to the end of tape.

Corrective action for this condition is to inform the user's program of this condition. If writing to tape, the user's program should write an end of volume mark (two tape marks) and then rewind the tape. If reading from tape, the user's program should continue until an end of volume mark is read and then rewind the tape.

BIT 1:

1 = At load point (BOT)

0 = Not at load point

This bit indicates whether the tape is currently positioned at load point (beginning of tape). It is set upon the loading of the tape or after a rewind operation. It is cleared when a forward motion command is processed or when the tape is unloaded. When this bit is set the drive will reject backspace record and backspace file commands. When this bit is not set the drive will reject write format commands. If either of these conditions occur the command reject bit will be set, the command reject error class will indicate device reject, and register #5 will indicate either drive at BOT or drive not at BOT.

Corrective action for this condition is to inform the user's program.

BIT 0:

1 = At end of file (EOF)

0 = Not at end of file

This bit is set when the drive has detected an EOF on the tape during a read record, forward space record, or backspace record operation. This bit is also set upon successful completion of write file mark, forward space file, or backspace file operations. The end of file is also known as a tape mark or a file mark.

Corrective action for this condition should be to inform the user's program.

Word 0, Byte 2 (Status Register #2)

BIT 8	BIT 9	BIT 10	BIT 11	BIT 12	BIT 13	BIT 14	BIT 15
6250 GCR format	Unknown Density	Data Parity Error	Data Timing Error	Tape Runaway	Door Open	Long Record Support	I.R. Mode

BIT 15:

1 = Immediate response mode.

0 = Non-immediate response mode.

This bit indicates whether immediate response to write operations is enabled. This bit is set when an enable_immediate_response mode command is received and accepted. This bit is cleared when a disable_immediate_response mode command is received and accepted, or when a tape is unloaded. The default mode at power up is that this bit is cleared.

BIT 14:

1 = Long records supported

0 = Long records not supported

This bit indicates that records up to 32K in PE and 60K in GCR are supported. If not set the maximum is 16K. The HP 7978B, 7979A/S, and 7980 set this bit, all other drives do not.

BIT 13:

1 = Door open

0 = Door not open

This bit is set when the tape path door is open. It is cleared when the door is closed. This bit will only be set in a transparent status message (DSJ = 2).

BIT 12:

1 = Tape runaway

0 = Not tape runaway

This bit indicates that the drive has read approximately 4.6 meters (15 ft) GCR tape, or 7.6 meters (25 ft) of PE or NRZI tape, without detecting a recorded block. At this point tape motion will stop. Tape runaway is detected for read record and on all space type commands.

Corrective action for this condition should be to inform the user's program. The user's program should issue the appropriate commands to move the tape where data is recorded. This is normally done with either the rewind, the backspace record, or the backspace file command.

BIT 11:

1 = Data timing error

0 = No data timing error

This bit indicates when a read or write timing error (overrun/underrun) has occurred. Because of the tape drive's data buffer this condition should never occur.

BIT 10:

1 = Data parity error

0 = No data parity error

This bit indicates when data parity error on the drive's internal data bus has been detected. This error can exist on any read record or write record operation. The drive will have completed all possible retries.

Corrective action for this condition should be to issue a backspace record command and then reissue the failed command. If this error persists then there is a hardware problem and the service man should be called.

BIT 9:

1 = UNKNOWN density detected

0 = not UNKNOWN density

This bit will be set when the drive cannot identify the tape as GCR, PE, or NRZI, and the tape is not blank. This bit will be also be set if the density on the tape is not available on the drive. This bit will be cleared when the tape is unloaded or by setting the drive to GCR, PE or NRZI with a valid wrote mode command while at load point. This bit will also be set along with the GCR format bit when reporting a hard error on a data compressed tape.

BIT 8:

1 = GCR (6250 BPI) format

0 = Not GCR format

This bit is set upon the identification of a GCR tape or the setting of the tape drive into the GCR format at load point.

When this bit is cleared there could be no tape loaded or the tape loaded is PE, NRZI, blank, or an unknown density. This bit can only be set by the HP 7978A, 7978B, and 7980.

Word 1, Byte 1 (Status Register #3)

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1600 PE format	800 NRZI format	Power Just Restored	HP-IB Command Parity Error	Position Unre-covered	Format-ter Error	Servo Error	Contrl. Error

BIT 7:

1 = Controller error

0 = No controller error

This bit indicates that the drive has detected an error in its controller. Register #5 will elaborate on this error condition.

Corrective action for this condition should be to log this error and call service if the failure persists.

BIT 6:

1 = Servo error.

0 = No servo error.

This bit indicates that the drive has detected an error in its servo subsystem. Register #5 will elaborate on this error condition.

Corrective action for this condition should include a visual inspection of the drive by the operator. A poorly loaded tape or defective could cause this error. This error should be logged and the service called if necessary.

BIT 5:

1 = Formatter error.

0 = No formatter error.

This bit indicates that a hardware error has been detected on the drive's formatter board or subsystem. Register #5 will elaborate on this error.

Corrective action for this condition should be to log this error and call service if the error persists.

BIT 4:

1 = Position unrecovered

0 = Position known and correct

This bit will be set when position on the tape (media) is no longer known. Normally, even on an error condition, the tape is positioned to a known place. However, it is possible for the drive to lose its place in which case this bit will be set. The tension shutdown circuitry will also cause this error. If tape tension is lost the drive will go offline.

BIT 3:

1 = HP-IB command parity error

0 = Correct parity

This bit indicates that the drive's ABI chip has detected a parity error in a HP-IB command byte. These commands include primary bus commands, secondary address bus commands, and universal bus commands. Normal command parity is an odd number of 1's on the DIO lines 1 thru 8.

Corrective action for this condition should be to log the condition. If this error persists, the service man should be called.

BIT 2:

1 = Power has been restored

0 = Normal power condition

This bit is set to 1 whenever power is applied to the drive, either during the normal power up sequence with the on/off switch or during a power fail/recovery sequence. This bit is also set immediately following the execution of a device clear.

Corrective action should be to undergo the power up protocol sequence.

BIT 1:

1 = NRZI (800 BPI) format

0 = Not NRZI format

This bit is set upon the identification of a NRZI tape or the setting of the tape drive into the NRZI format at load point. When this bit is cleared, no tape is loaded or the tape loaded is GCR, PE, blank, or an unknown density. This bit can only be set by an HP 7974A with the 800 NRZI option.

BIT 0:

1 = PE (1600 BPI) format

0 = Not PE format

This bit is set upon the identification of a PE tape or the setting of the tape drive into the PE format at load point. When this bit is cleared, no tape is loaded or the tape loaded is GCR, blank, or an unknown density.

Word 1, Byte 2 (Status Register #4)

BIT 8	BIT 9	BIT 10	BIT 11	BIT 12	BIT 13	BIT 14	BIT 15
Error class (3 bits) (3 bits)			Physical retry count (5 bits)				

BITS 11-15: Retry Count

These five status bits indicates the number of retries performed by the tape drive. These bytes are the same as for the 7976.

0	Successful operation complete on first try.
1	Correctable error detected on first try.
>1	Number of tries to finally complete the operation, where the success or failure is indicated elsewhere.

BITS 8-9: Error class

These status bits indicate the reason for a command reject error.

0 = No command reject.

1 = Reserved.

2 = Device reject (register #5 contains the reject code).

3 = Protocol reject (register #5 contains the reject code).

4 = Reserved.

5 = Reserved.

6 = Reserved.

7 = Selftest failure.

Word 2, Byte 1 (Status Register #5)

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Error code (8 bits)							

The contents of this register is dependent on the particular error being reported.

If command reject (STATUS REG. #1, BIT 4) is asserted and register #4 indicates a device reject, this register defines the specific error condition as follows:

5	Device is write protected when a write type command was initiated.
6	Tape was not loaded when the command was received.
7	Write density command given but the requested density is not available.
9	The tape to be read was unidentifiable as to format. The density read may not be available, or the tape may have an unreadable density ID, or may be blank.
10	The tape to be written is unidentifiable as to format. A Write Record, Write File Mark, or Write Gap command was received but cannot be processed without a Write Format command if the tape was unidentified at load point.
11	Drive not online.
16	A write format command was issued but the tape is not positioned at BOT.

19	A backward type command (except rewind) was just initiated but the tape was already positioned at BOT.
23	Protocol not synced (Host issued a tape command prior to responding to the device's power-on parallel poll).
24	The tape command byte received was unknown to the drive.
31	The length of a write record requested exceeded the maximum record size supported by the drive.
33	Selftest failure. Drive will not accept tape commands.
37	Tape positioning failure while removing readaheads.
40	Door open reject. The door was opened during a long gap while the tape was beyond the end of tape marker. This condition is non-retriable to prevent unspooling of the tape.

If unrecovered data/format error (STATUS REG. #1, BIT 6) is asserted this register specifies the particular error encountered. The status is defined as:

41	The tape velocity was out of specification.
45	Multiple tracks were in error. Either two or more tracks were in error for a PE or NRZI write, or two or more tracks were in error for a GCR write.
47	Failure to verify a tape mark or density ID just written.
48	Noise on detect. Indistinguishable flux transitions were detected while attempting to detect a recorded block.
49	Data format error. Flux transitions were found or were missing in the appropriate tracks for a block detect.
50	Failure to identify tape following a rewind command.
51	Gap detected before end of data. The read formatter detected a full tape width dropout within the data portion of a data block.
52	Data block dropout. A full tape width dropout was detected within the preamble or postamble of a data block.
53	Redundancy check error. The read formatter detected either a CRC, ACRC, LRC, or residual error while reading or verifying a data block.
54	Read parity error. The read formatter detected an unrecovered parity error within a data block. For PE this error could include multiple tracks in error, and for GCR this error could also include a redundancy check error. (7978B, 7979A/S, 7980 only).
55	Abnormal command abort, door opened.
57	(HP 7974A only) Maximum skew exceeded.
58	(HP 7974A only) False preamble or postamble detected.
59	Corrected data error on write.
60	Buffer overrun. The record size exceeded the maximum record size supported on a read.

61	Data block timeout. Could not detect the gap following a data block. Could be caused by a record length longer than what the drive supports on read.
62	Tape mark dropout. A full tape width dropout was detected within a tape mark.
63	Tape mark unverified. A tape mark was detected which does not meet ANSI specifications in terms of flux transitions and erasure in the appropriate tracks.
64	Tape mark timeout. Could not detect the gap following a detected tape mark.

If position unrecovered (STATUS REG. #3, BIT 4) or Servo error (STATUS REG. #3, BIT 6) is asserted, this register will define the specific error condition as follows:

81	Servo controller unresponsive. The servo will not take data from the master controller.
82	Servo failed to reach the desired state requested by the master controller.
83	Servo shutdown. The servo system lost tape tension unexpectedly.
84	Servo controller hard failure. The servo controller has detected a hard failure within itself.
85	Servo protocol error. An invalid byte was received by the servo from the master controller.
86	A run time error was detected by the servo.
87	In position interrupt not received. Master controller did not get the in position interrupt it expected.
88	No gap detected by the servo after reading or writing a data block or tape mark.
89	Safety shutdown of motor driver.
90	No BOT detected on load or rewind.
91	Speed out of specifications.

92	The desired state requested by the master controller was invalid for the current context.
94	Tape positioning failure.

If a Formatter error (STATUS REG. #3, BIT 5) is asserted this register defines the specific error condition as follows:

101	7978 Read Formatter unresponsive. The read formatter did not respond with end of record status after a data block was detected.
102	7978 Read Formatter hardware error.
103	Bad block type detected on a write operation.
104	Erase failure. Flux transitions were detected in a portion of tape currently being erased.
105	No data detected after write.
106	Tracks out of sync on write verify.
107	(HP 7974A only) Formatter hardware error.
108	(HP 7974A only) Formatter unresponsive.
109	No gap timeout. The gap timer did not count down, or was never started.
110	Formatter byte count mismatch with data buffer.
U	

If controller error (STATUS REG. #3, BIT 7) is asserted this register indicates the specific error condition as follows:

121	Transaction ID mismatch between command sent to Device program and the returned report.
122	No pending command found for report received from Device program.
123	Invalid report message received from Device program.
124	Report queue overflow.
125	Unknown command received by Device program.
126	Command queue overflow.
128	Missing End Of Record flag in data buffer.
129	Data buffer parity error.
130	Data buffer underrun during a write operation
131	Byte count mismatch between putting a record into the data buffer and removing it.
132	Bad message type received by channel program from device program.
133	Processor handshake abort between HP-IB interface board and channel program.
134	Unknown HP-IB interface exception detected.
137	Illegal access to the servo controller registers detected.
138	Device program firmware error.
139	Hardware utilities firmware error.
140	Channel program firmware error.
141	One line encoder inoperative.
150	Tape position synchronization error (HP7980XC/SX only).
151	Tape deblocking error (HP7980XC/SX only).

152	Compression/decompression hardware/firmware error (HP7980XC/SX only).

If command reject (STATUS REG. #1, BIT 4) is asserted and Status Register #4 indicates a protocol error, this register defines the specific error condition as follows:

161	Command queue not empty. Cannot accept new tape command or diagnostic request.
162	Request DSJ expected
163	Request status expected
165	Unknown unit select.
166	Tape command secondary expected.
167	Data byte expected.
168	Missing EOI on tape command data byte, selftest number, or END command data byte.
170	Command phase protocol error for write record.
172	Read record report phase protocol error.
173	Report phase protocol error.
174	Cold load sequence protocol error.
175	HP-IB protocol sequence error.
176	END "COMPLETE" or "COMPLETE-IDLE" expected.
178	END "DATA" expected.
180	Unknown interface secondary command.
181	Misplaced data byte.
184	Interface loopback protocol error.
185	Run selftest protocol error.
188	HP-IB command parity error.
189	Reset by operator during a protocol sequence.
190	Device clear received. (Internal error code only).
254	All reserved CCL error codes (see "7979A/S/7980A/S Error Cross Reference" after these Status Decodes)

(254) CCL Error Codes 94,95 *** revision 3.40 and earlier firmware return these errors here. They should be mapped to HP-IB error #47, and will be fixed in the future.

255 CCL Error Codes 3, 5, 7, 8, 9, 14, 18, 19, 20, 21, 23, 28, 29, 30, 31, 117 (see "7979A/S/7980A/S CCL Errors" after these Status Decodes)

Word 2, Byte 2 (Status Register #6)

BIT 8	BIT 9	BIT 10	BIT 11	BIT 12	BIT 13	BIT 14	BIT 15
Back Reference Count (8 bits)							

This register is used only when reporting transparent status of hard and soft errors while in immediate response mode. When an immediate reported write has a soft error (retries were necessary) or a hard error (write failure) this register indicates which command had the error. It contains the number of commands sent and reported since the command in question was issued. If the immediate reported write had a hard error all of the commands issued after the failure also fail (they will be aborted). Thus on a hard error this register actually indicates the number of preceding commands that failed.

9

Replaceable Parts

In this chapter you will find the following information:

- An explanation of FRU part numbering
- A table of parts including
  - Exchange parts
  - Non-exchange parts
  - Miscellaneous screws
  - Cabinet hardware
  - Firmware kits
  - 88780A/B exclusive parts
- Special material considerations
- Exploded-view drawings of the 1/2-inch Tape Drive

9.1 FRU Part Numbering

Table 9-1. FRU Part Numbering

Part Number Structure	Type of FRU	Example
xxxx-xxxx (four-by-four)	Purchased part. This is a manufacturing number only.	1390-0776 Cover Latch
xxxxx-xxxxx	Special Service Part designations of a part number will be a five-by-five number. The second five numbers of the number show whether a FRU is original equipment, an exchange part, or sometimes indicate a revision. Depending on the service history of the device, all of these numbers may be seen on a FRU. The following explains the meaning of the different sequences of numbers that may be on a FRU.	
xxxxx-665xx	FRU fabricated by Greeley	xxxxx-66509
xxxxx-677xx	FRU that is an assembly	xxxxx-67709
xxxxx-679xx	FRU that is an assembly	xxxxx-67909
xxxxx-60xxx	Service designation for a new part	xxxxx-60x09
xxxxx-601xx	Third number indicates a major revision of the FRU.	xxxxx-60109
xxxxx-69xxx	Service designation for an exchange part	xxxxx-69x09
xxxxx-691xx	Third number indicates a major revision of the FRU.	xxxxx-69109

Options and the Main FRUs

Cardcage Slot #1 (4-FRU Versions)

Table 9-2. Cardcage Slot #1 (4-FRU Versions)

FRU Description	Replacement Part Number	Notes
Read/Write/ PLL FRU	07980-69001	For 4-FRU versions - prior to serial number prefix 2805A for the 7979A and 2806A for the 7980A

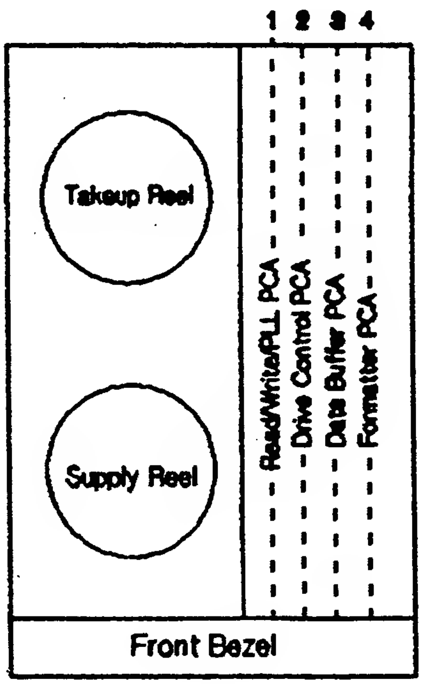


Figure 9-1. Four FRU Version of the Drive (earlier version)

Cardcage Slot #1 (3-FRU Versions)

Table 9-3. Cardcage Slot #1 (3-FRU Versions)

FRU Description	Replacement Part Number	Notes
Read/Write/ Formatter/PLL FRU	88780-6xx21	For 3-FRU versions - serial number prefix 2805A and later for the 7979A and 2806A and later for the 7980A
	88780-69121	If GCR, PE
	07980-60031	If Option 800

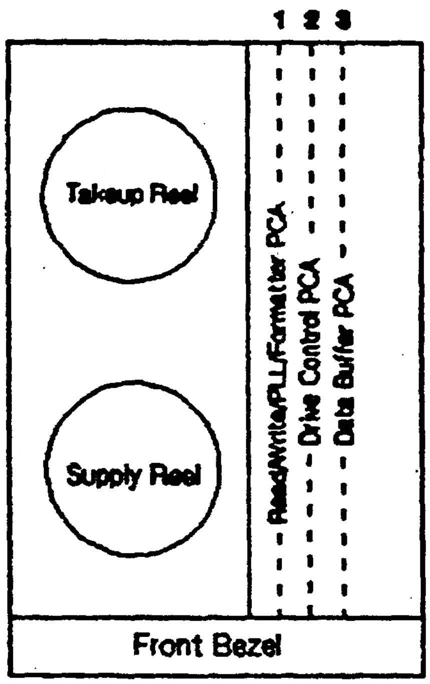


Figure 9-2. Three FRU Version of the Drive (later version)

Cardcage Slot #2

Table 9-4. Cardcage Slot #2

FRU Description	Replacement Part Number	Notes
Drive Controller FRU	07980-6xxx3	
	07980-69203	If 6250 bpi (7980A, 7980XC)
	07979-69213	If 1600 bpi (7979A)

Cardcage Slot #3

Table 9-5. Cardcage Slot #3

FRU Description	Replacement Part Number	Notes
Data Buffer FRU	07980-6xxx4	
	07980-69004	If 7980A S/N 3021Axxxxx or below
	07980-60034	If 7980A S/N 3121Axxxxx or above
	07980-60034	If Option 800 (7979A, 7980A)
	07980-69024	If 7980XC or 88780 Option 400
	07980-60034	If 1 Mbyte Cache

Cardcage Slot #4 (4-FRU Versions)

Table 9-6. Cardcage Slot #4 (4-FRU Versions)

FRU Description	Replacement Part Number	Notes
Read Formatter FRU	07980-69002	For 4-FRU versions prior to serial number prefix 2805A for the 7979A and 2806A for the 7980A

9.2 Parts List

Note In the following list "x"s are used as placemarkers in FRU numbers. All "x"s are 0 to 9. To determine a part number at the time you are servicing the unit, look up the part number with a "0" in place of the "x". If a NEW part number exists, it will be cross-referenced.

Table 9-7. 1/2-inch Tape Drive Parts List

FRU Number	Drawing Number	Part Number	Description
Exchange Parts (Refer to Figures 9-3 and 9-4 for Drawing Numbers			
01	1	07980-69x01	Rd/Wrt/PLL FRU
02	4	07980-69x02	Read Formatter FRU
21	1	88780-69121	Rd/Wt/PLL/Format FRU
03	2	07980-69x03	7980A/88780A/B Controller FRU
04	3	07980-69x04	Data Buffer FRU
05	5	07980-69x05	Motor/Power FRU
07	9	07980-69x07	HP-IB Interface FRU
13	2	07979-69x13	7979A Controller FRU
05	5	88780-69x05	Motor/Power FRU -IEC 950 (only 88780A/B)
14	3	07980-69x14	Substitute 07980-60x34 (non-exchange)
24	3	07980-69x24	Data Buf.FRU w/Data Comp.

Table 9-7. 1/2-inch Tape Drive Parts List (continued)

FRU Number	Drawing Number	Part Number	Description
Non-Exchange Parts			
	7	07980-61618	Standby Power Switch Assembly
	8	07980-44111	Standby Power Switch Button
08	10	07980-60x08	Front Panel FRU
09	11	07980-60x09	Tape Sensor Assembly
31	1	07980-60x31	800 cpi Rd/Wrt/PLL FRU
34	3	07980-60x34	Data Buffer, 1 Mbyte
	9	88780-60x35	SCSI Single-Ended Interface
41	12	07980-60x41	Speed Sensor Assembly
41		07980-60x48	NRZI Speed Sensor
40	13	07980-60040	EOT/BOT Sensor Assembly
44	30	07980-60244	Hub Lock
	15	07980-60x53	Supply Hub Assembly
		07980-60046	Slide Rails (pair)
45	16	07980-60x45	Buffer Arm Assembly
51	17	07980-60x51	Tape Displacement Unit
54(42)	14	07980-60054	Head Plate Assembly
62		07980-60062	Speed Sensor Cable
64		07980-60064	Front Panel Cable
65		07980-60065	Motor Control Cable
		07980-60066	Front Panel Microswitch Cable
67		07980-60167	Interface Cable
70		07980-60070	Wiring Harness
71		07980-60071	Read Head Cable
72		07980-60072	Write Head Cable
	18	07980-60049	Door Latch Assembly
	19	1390-0776	Cover Latch
	20	1420-0314	3-volt Battery
	21	07980-48316	Blower Fan Duct

Table 9-7. 1/2-inch Tape Drive Parts List (continued)

FRU Number	Drawing Number	Part Number	Description
		2680-0308	Motor Hub Screw—Screw, machine, 10-24x0.50, T25, 82-degree pan, hardened. Older drives may have 10-24x0.625, T20, 82-degree flathd. Use new screw.
		2680-0305	Screw, 10-24x0.625, T25, pan taptite
	24	3110-0178	Cover Hinge
	25	07980-60043	Cooling Fan
		07980-81901	Door Microswitch
	27	1460-2180	Buffer Spring
	28	07980-67919	Power Module
	29	07980-60x00	Motherboard FRU
	30	07980-60x44	Hub Lock Assembly
	31	07980-60x47	Front Bezel Assembly
	32	07980-60x52	Takeup Hub Assembly (hub and flange)
50	33	88780-60049	Takeup/Supply Reel Motor
		07980-48312	Reel Encoder Flag (for Supply Hub)
		07980-48323	Write Encoder Flag (for Supply Hub)
		07980-48311	Foot Pad (for Reel Lock Feet)
	34	07980-86500	Blower Motor (Load Fan)
	35	9100-4637	Transformer
	36	07980-44105	Top Cover
	37	2110-0056	6-Amp Fuse
	38	2110-0655	3.5-Amp Fuse
	39	07980-40600	Shroud
		0515-0951	Screw, M2.5x0.45x16, Posidriv, pan
		3101-2917	Front Panel Function Switches (8)

Table 9-7. 1/2-inch Tape Drive Parts List (continued)

FRU Number	Drawing Number	Part Number	Description
Miscellaneous Screws			
		0515-1125	Screw, M3.0x0.50x10, Pozidriv, 90-degree flathead, w/patch lock
		0515-0459	Screw, M4.0x0.70x12, Pozidriv, pan,w/tooth washer
		0515-0935	Screw, socket,M4.0x0.70x40, hexhd cap
		0624-0615	Screw, 2-28x0.562, T7, pan
		0624-0620	Screw, 4-20x0.25, T9, pan, plastic tapping
		2200-0139	Screw, 4-40x0.250, Pozidriv, pan, w/sq.cone washer
		0624-0690	Screw, tapping, 4-40x0.250,T10, Taptite
		2200-0757	Screw, 4-40x0.688, Pozidriv, pan
		2360-0113	Screw, 6-32x0.250, Pozidriv, pan w/tooth washer
		2360-0119	Screw, 6-32x0.438, Pozidriv, pan w/tooth lockwasher
		2360-0297	Screw, 6-32x0.438, Pozidriv, pan, (cardcage, interface assys)
		2680-0281	Screw, 10-32x0.375, T25, pan w/lockwasher
		2680-0320	Screw, 10-32x0.75, T25, pan w/lockwasher
Cabinet Hardware			
		07980-00210	Option 137 Bottom Panel
		07980-00201	Standard Door
		07980-60058	Hinge/Catch Kit
		07980-60057	Cabinet
		07980-67191	Cabinet Side Panel
		07980-67192	Cabinet Back Door
		07980-67193	Cabinet Top Cover
		07980-67194	Cabinet Lock and Key
		07980-00207	Dual-drive rack filler panel

Table 9-7. 1/2-inch Tape Drive Parts List (continued)

FRU Number	Drawing Number	Part Number	Description
Firmware Kits			
		07980-60x90	7979/7980 3.xx FW Kit (HP-IB)
		07980-60x91	6.xx FW Kit (HP-IB)
		07980-60x92	7980S/SX FW Kit (SCSI)
88780A/B			
5	5	88780-69x05	Motor/Power FRU
15	9	88780-60x35	SCSI single-ended interface
16	9	88780-60x36	SCSI differential interface
22	9	88780-69x22	Pertec-compatible interface
		88780-60095	Loopback Conn. SCSI Sgl-end.
		88780-60096	Loopback Conn. SCSI Diff.
		88780-64x00	88780/SCSI CCLII FW Kit (Rev. 6.xx)
		88780-64x01	88780/Pertec CCLII FW Kit (Rev. 6.xx)
		88780-04400	Desktop Enclosure cabinet (used with HP 88780A, full kit is HP 88706A)
		88780-04710	Desktop Enclosure cabinet (hidden hinge, used with HP 88780B)

Special Material Considerations

While no special tools are required to service the 7979/7980/88780 drives, there are items commonly used for all 1/2-inch tape drives. For the purpose of reference, a master skew tape (HP part no. 9162-0027) should be stocked and available as an area resource.

A logic analyzer, such as a 1630x, is recommended to be available for use by CEC personnel. But such a tool is not required nor necessary for normal support use.

Removal of the Motor Power FRU (07980-69x05 or 88780-69x05) is easier if a Torx extension is used (8710-1425 or equivalent).

9.3 Exploded-View Drawings

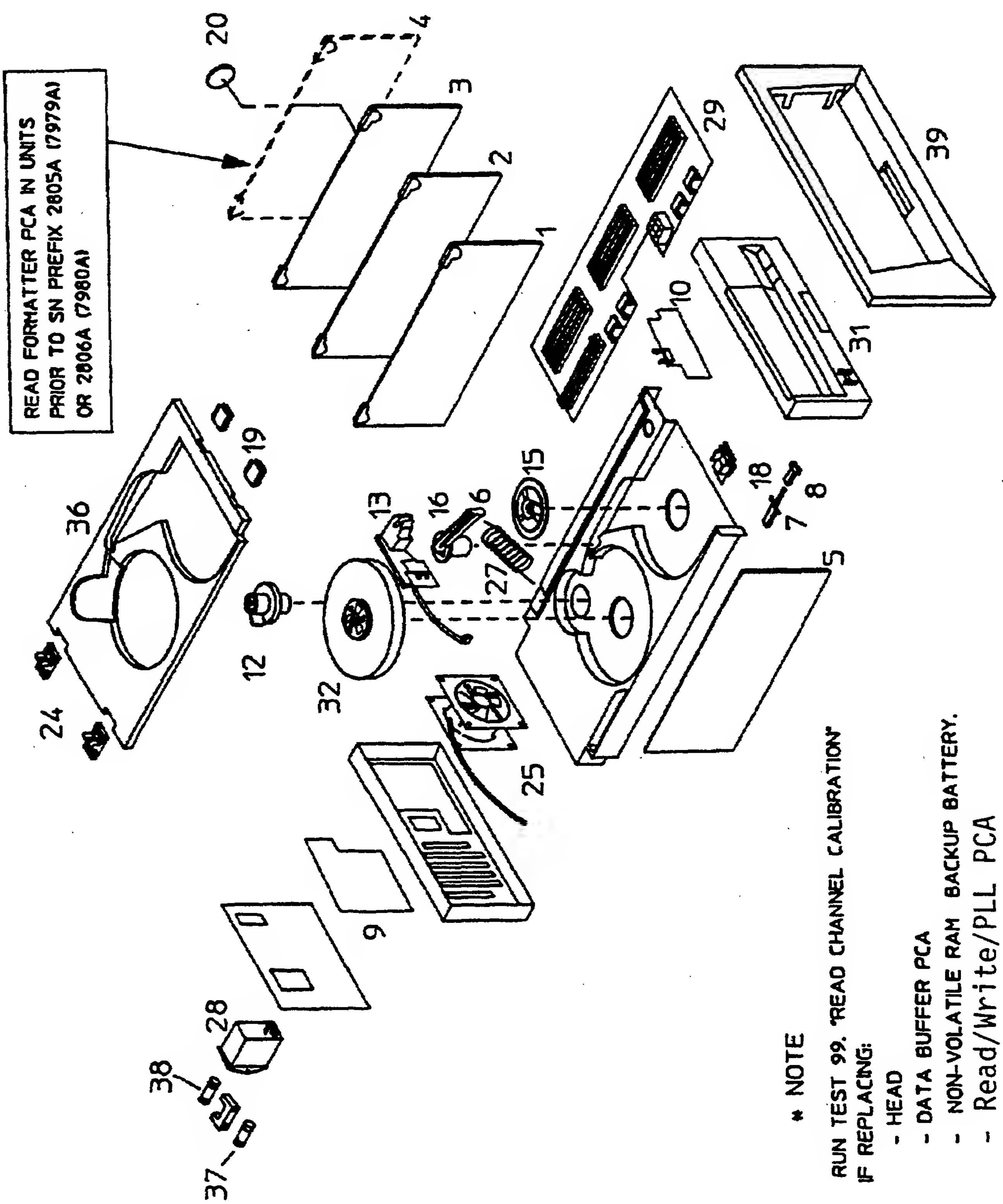


Figure 9-3. Exploded View (1 of 2)

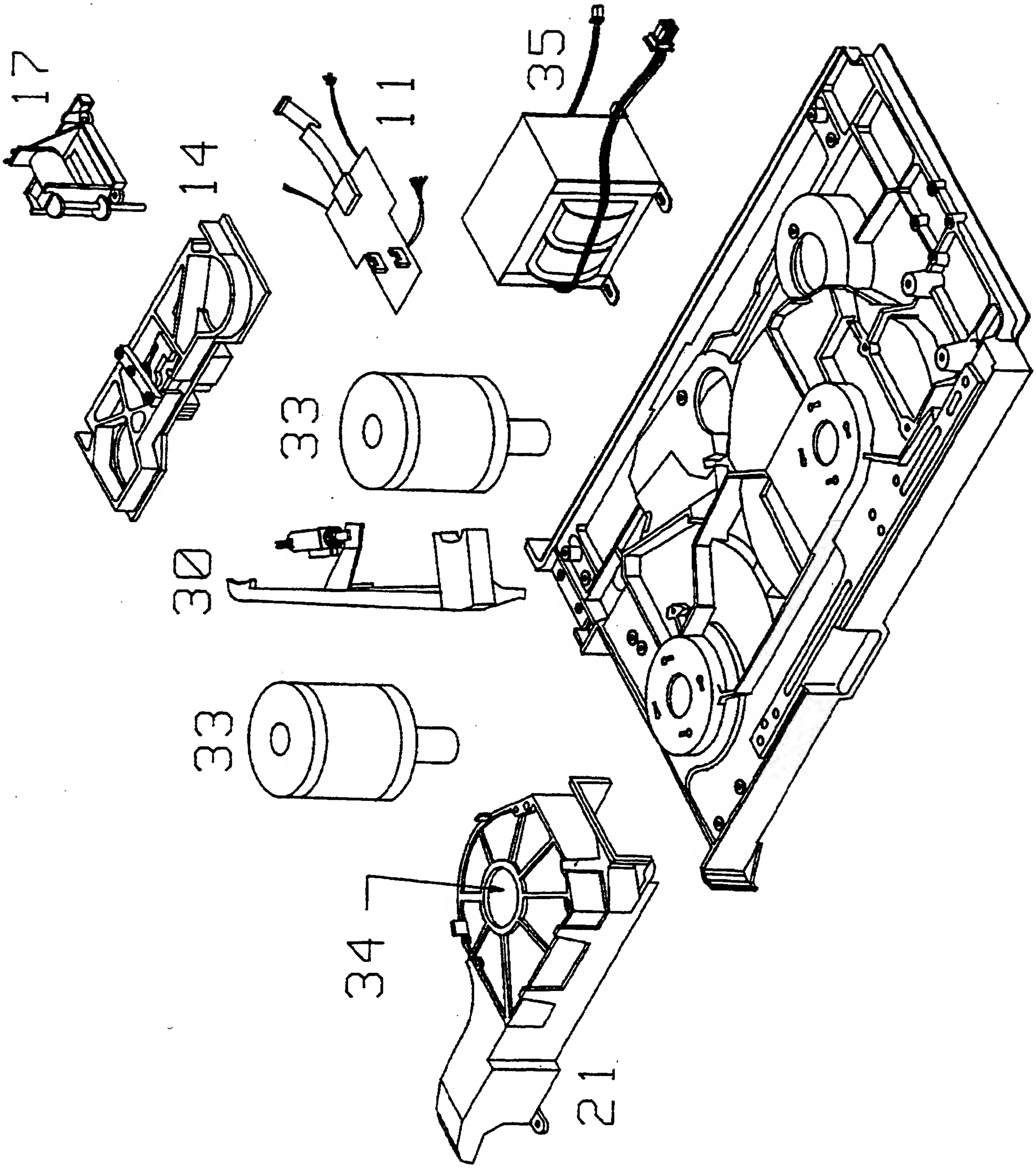


Figure 9-4. Exploded View (2 of 2)

10

References

None designated at this time.

11

Product History

Table 11-1. 7979A Product History

Change	Service Note Date	Serial Number
Front Panel Bezel coated with RFI-reducing nickel-impregnated paint. See SN 7979A-1..	10/87	2729A and above
Firmware update. Improves performance with small records and operations involving the Tape Displacement Unit, hub lock, autoload, and the Front Panel. See SN 7979A-2.	10/87	2729A and above
Hub Lock Assembly changed to improve process of manufacture and reliability. See SN 7979A-3.	10/87	2729A and above
Standby Switch Assembly replaced with a new version. See SN 7979A-4.	10/87	2730A and above
Read/Write/PLL PCA and Read Formatter PCA combined into a single Read/Write/Formatter/PLL PCA (07980-60021). See SN 7979A-5.	3/88	2805A and above
Firmware update. Rev. 3.4 to 3.5. Code changes for the Drive Control, Data Buffer, and HP-IB PCA. Adds support for the Read/Write/Formatter/PLL PCA (07980-60021) in addition to the previous Read/Write/PLL PCA (07980-60001) and the Read/Formatter PCA (07980-60002). See SN 7979A-6.	3/88	2805A and above

Table 11-1. 7979A Product History (continued)

Change	Service Note Date	Serial Number
Takeup hub assembly modified to reduce tape leader foldovers. See SN 7979A-7.	3/88	2729A00629 and above
New rotating slide rails. See SN 7979A-8	5/88	2807A01088 and above
Power/Motor PCA (07980-60005) modified to improve RFI noise margin. See SN 7979A-9.	6/88	2807A01200 and above
Read/Write/Formatter PCA (07980-60021) modified and part number changed to 07980-60121. See SN 7979A-10.	7/88	2807A00741 through 2807A01225
Procedures for possible physical hazard using rotating slides. See SN 7979A-11B-S . (supersedes SN 7979A-11, 8/88 and SN 7979A-11A-S, 11/88)	11/88	2807A01088 to 2807A01339
Possible electrical shock hazard using some power plug configurations with a 7936/37 disk drive in same cabinet. See SN 7979A-12.	8/88	ALL
800 BPI density supported by Option 800. See SN 7979A-13.	9/88	N/A
New interface cable improves noise immunity. See SN 7979A-14.	11/88	2807A01638 and below
New Buffer Arm Friction Clip available. See SN 7979A-15.	11/88	N/A

Table 11-1. 7979A Product History (continued)

Change	Service Note Date	Serial Number
Modifications for improving general reliability of the 7979A See SN 7979A-16	1/90	2807A03354 and below
A new firmware update kit restores lost NRZI skew values See SN 7979A-17A (supersedes 7979A-17)	10/89	0000A00000 through 2807A02934
New buffer arm to fix excessive media dependent misloads See SN 7979A-18	10/89	2816A00370 through 2816A01380
A change was made to the Front Panel PCA to improve the reliability of the Front Panel Switches. See SN 7979A-19	1/90	2807A00000 through S807A02060
The specified drives may write NRZI tapes that do not meet ANSI specifications. See SN 7979A-20	3/90	2807A03059, 2807A03101, 2807A03113, 2807A03130, 2807A03138, 2807A03319, 2807A03348, 2807A03384
New and refurbished buffer PCAs will be shipped with non- replaceable batteries. See SN 7979A-21	8/90	0000A00000 through 9999Z99999
A new firmware revision kit (3.88) is available that corrects several product reliability problems. See SN 7979A-23	11/90	0000A00000 through 3020A03863

Table 11-2. 7980A Product History

Change	Service Note Date	Serial Number
Front Panel Bezel painted with RFI-reducing nickel-impregnated paint. See SN 7980A-1.	10/87	2730A and above
Firmware update. Improves performance with small records and operations involving the Tape Displacement Unit, hub lock, autoload, and the Front Panel. See SN 7980A-2.	10/87	2730A and above
Hub Lock Assembly changed to improve manufacturability and reliability. See SN 7980A-3.	10/87	2730A and above
Standby Switch Assembly replaced with a new version. See SN 7980A-4.	10/87	2730A and above
Read/Write/PLL PCA and Read Formatter PCA combined into a single Read/Write/Formatter/PLL PCA (07980-60021). See SN 7980A-5.	2/88	2806A and above
Firmware update. Rev. 3.4 to 3.5. Code changes for the Drive Control, Data Buffer, and HP-IB PCA. Adds support for the Read/Write/Formatter/PLL PCA (07980-60021) in addition to the previous Read/Write/PLL PCA (07980-60001) and the Read/Formatter PCA (07980-60002). See SN 7980A-6.	2/88	2806A and above
Takeup hub assembly modified to reduce tape leader foldovers. (See SN 7980A-7.	3/88	2730A51748 and above
New rotating slide rails. See SN 7980A-8.	5/88	2806A53199 and above
Power/Motor PCA (07980-60005) modified to improve RFI noise margin. See SN 7980A-9.	6/88	2806A53652 and above

Table 11-2. 7980A Product History (continued)

Change	Service Note Date	Serial Number
Read/Write/Formatter PCA (07980-60021) modified and part number changed to 07980-60121. See SN 7980A-10.	7/88	2806A52042 through 2806A53742
Procedures for possible physical hazard using rotating slides. See SN 7980A-11B-S. (supersedes SN 7980A-11, 8/88 and SN 7980A-11A-S, 11/88)	11/88	2806A53199 to 2806A54129
Possible electrical shock hazard using some power plug configurations with a 7936/37 disk drive in same cabinet. See SN 7980A-12.	8/88	ALL
800 BPI density supported by Option 800. See SN 7980A-13.	9/88	N/A
New interface cable improves noise immunity. See SN 7980A-14.	11/88	2806A54910 and below
New Buffer Arm Friction Clip available. See SN 7980A-15.	11/88	N/A

Table 11-2. 7980A Product History (continued)

Change	Service Note Date	Serial Number
Modifications for improving the general reliability of the 7980A See SN 7980A-16	1/90	2806A58872 and below
New firmware kit which eliminates a potential data corruption problem, a potential field "skew adjustment" failure, and a failure to ID 800 bpi tapes written on the 7974A. See SN 7980A-17	8/89	0000A00000 through 2806A57270
New firmware kit is available that restores lost NRZI skew values. See SN 7980A-17A (Supersedes 7980A-17.)	10/89	0000A00000 through 2806A58101
New buffer arm to fix excessive media dependent misloads See SN 7980A-18	12/89	2806A55965 through 2806A58402
A change has been made to the Front Panel PCA to improve the reliability of the Front Panel Switches. See SN 7980A-19	1/90	2806A00000 through 2806A55800
The specified drives may write NRZI tapes that do not meet ANSI specifications. See SN 7980A-20	3/90	2806A58391, 2806A58517, 2806A58518, 2806A58519, 2806A58524, 2806A58725, 2806A58743, 2806A58748, 2806A58759, 2806A58760, 2806A58769, 2806A58864, 2806A58869, 2806A58946

Table 11-2. 7980A Product History (continued)

Change	Service Note Date	Serial Number
New and refurbished Buffer PCAs will be shipped with non- replaceable batteries. See SN 7980A-21	8/90	0000A00000 through 9999Z99999
A modification is available that allows the decorative shroud to be permanently attached to the Front Bezel Assembly. See SN 7980A-22	10/90	0000A00000 through 9999Z99999
A new firmware kit (3.88) is available that corrects several product reliability problems. See SN 7980A-23	11/90	0000A00000 through 3021A59891
New door microswitch, front panel switch, door switch cable, front bezel assembly, door latch assembly, and hub lock assembly available. See SN 7980A-25	4/91	0000A00000 through 9999Z99999
A new display code, revision 6.40, is available. See SN 7980A-26	4/91	0000A00000 through 9999Z99999
Cable carrier for cabinets with a second drive installed. See SN 7980A-27	4/91	N/A
Correct noise problems with Pertec and SCSI interface drives. See SN 7980A-28	4/91	N/A

Table 11-3. 7980XC Product History

Change	Service Note Date	Serial Number
New Compression Buffer PCA available. (07980-60024). See SN 7980XC-1.	5/88	N/A
New family of firmware to support the 68000-based 07980-60024 Compression Buffer PCA. See SN 7980XC-2.	5/88	N/A
Introductory information about Data Compression operation and theory on the 7980XC. See SN 7980XC-3.	5/88	N/A
Procedures for possible physical hazard using rotating slides. See SN 7980XC-4B-S. (supersedes SN 7980XC-4, 8/88 and SN 7980XC-4A-S, 11/88)	11/88	2816A00100 to 2816A00131
Possible electrical shock hazard using some power plug configurations with a 7936/37 disk drive in same cabinet. See SN 7980XC-5.	8/88	ALL
New interface cable improves noise immunity. See SN 7980XC-6.	11/88	2816A00182 and below
New Buffer Arm Friction Clip available. See SN 7980XC-7.	11/88	N/A
Procedures for possible physical hazard using rotating slides. See SN 7980XC-8A-S. (supersedes SN 7980XC-8, 8/88)	11/88	2816A00131 and below
Modifications for improving general reliability of the 7980XC See SN 7980XC-9	1/90	2816A01270 and below

Table 11-3. 7980XC Product History (continued)

Change	Service Note Date	Serial Number
New buffer arm to correct excessive media dependent misloads See SN 7980XC-10	10/89	2816A00370 through 2816A01380
Change to the Front Panel PCA to improve the reliability of the Front Panel Switches See SN 7980XC-11	1/90	2816A00000 through 2816A00335
New and refurbished Buffer PCAs are shipped with non- replaceable batteries. See SN 7980XC-12	8/90	0000A00000 through 9999Z99999
New firmware kit (6.70) is available that corrects several product reliability problems. See SN 7980XC-14	11/90	0000A00000 through 2816A01847

Table 11-4. 7979S/7980S Product History

Change	Service Note Date	Serial Number
Introducing the 7979S, 7980S and 7980SX 1/2 inch SCSI interface streaming tape drive. See SN 7980S-1, 7979S-1, 7980SX-1	7/91	N/A

Table 11-5. 88780A/B Product History

Change	Service Note Date	Serial Number
Interface PCAs 88780-69010, 88780-69011, and 88780-69012 updated to 88780-69110, 88780-69111, and 88780-69112 repectively. See SN 88780A-1.	11/87	2712A and above
SCSI interfaces 88780-60110 and 88780-60111 obsoleted. Replaced with 88780-60016 and 88780-60015. See SN 88780A-2.	3/88	2815A and above
Firmware kits 88780-60090 and 88780-60092 obsoleted. Replaced with kits 88780-60290 and 88780-60292 with Revision 3.51. See SN 88780A-3.	3/88	2815A and above
Pertec-compatible interface 88780-60112 obsoleted. Replaced with 88780-60022. See SN 88780A-4.	3/88	2815A and above
Possible miswire on the Power Module. See SN 88780A-5.	11/88	2815A51310 and below
New motor/power PCA is available for 88780A/88780B tape drives. See SN 88780A-7 and 88780B-2	4/91	0000A00000 to 9999Z99999

12

Diagrams

Overall Block Diagrams

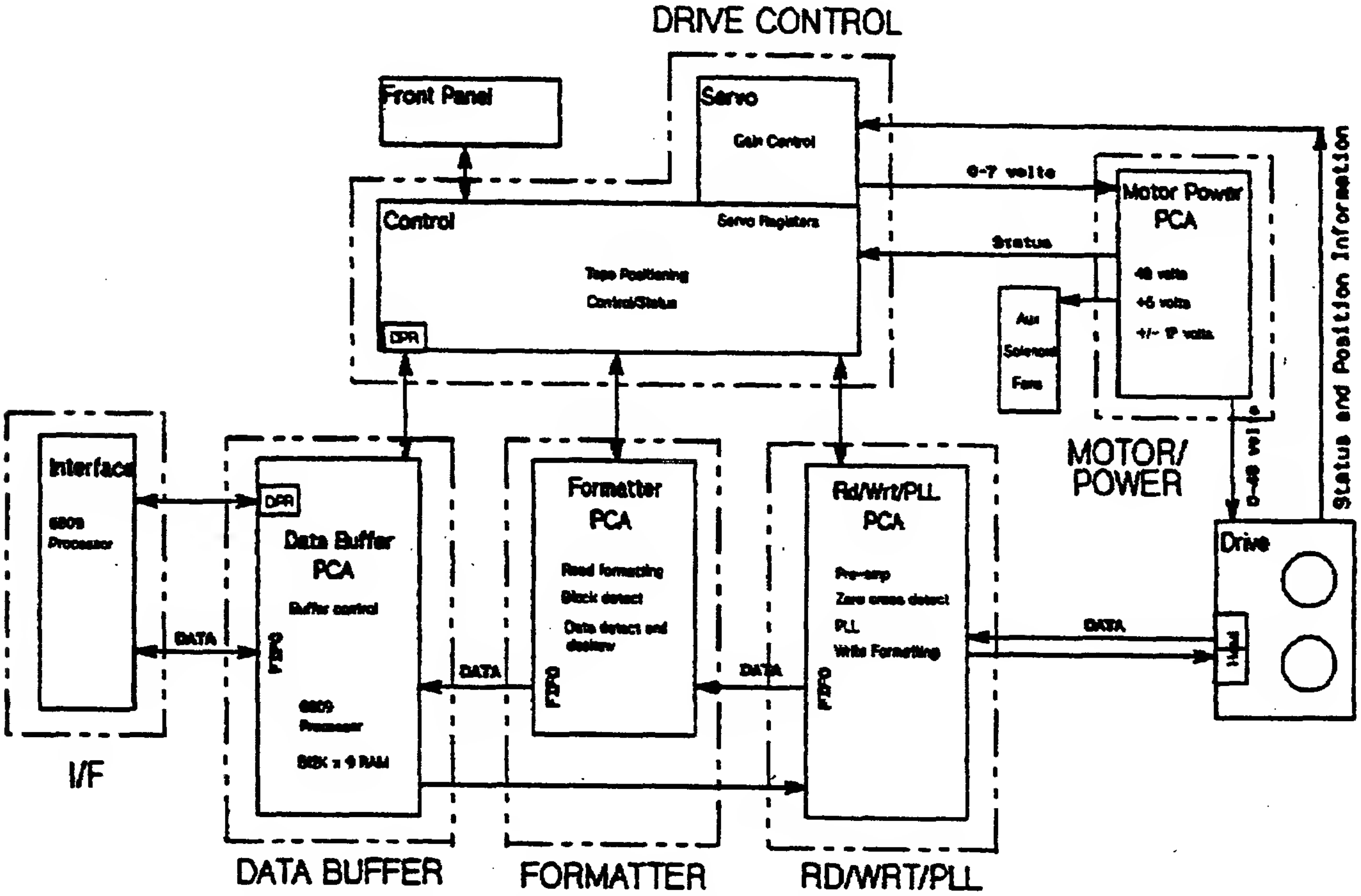


Figure 12-1. Overall Block Diagram (4-PCA Version)

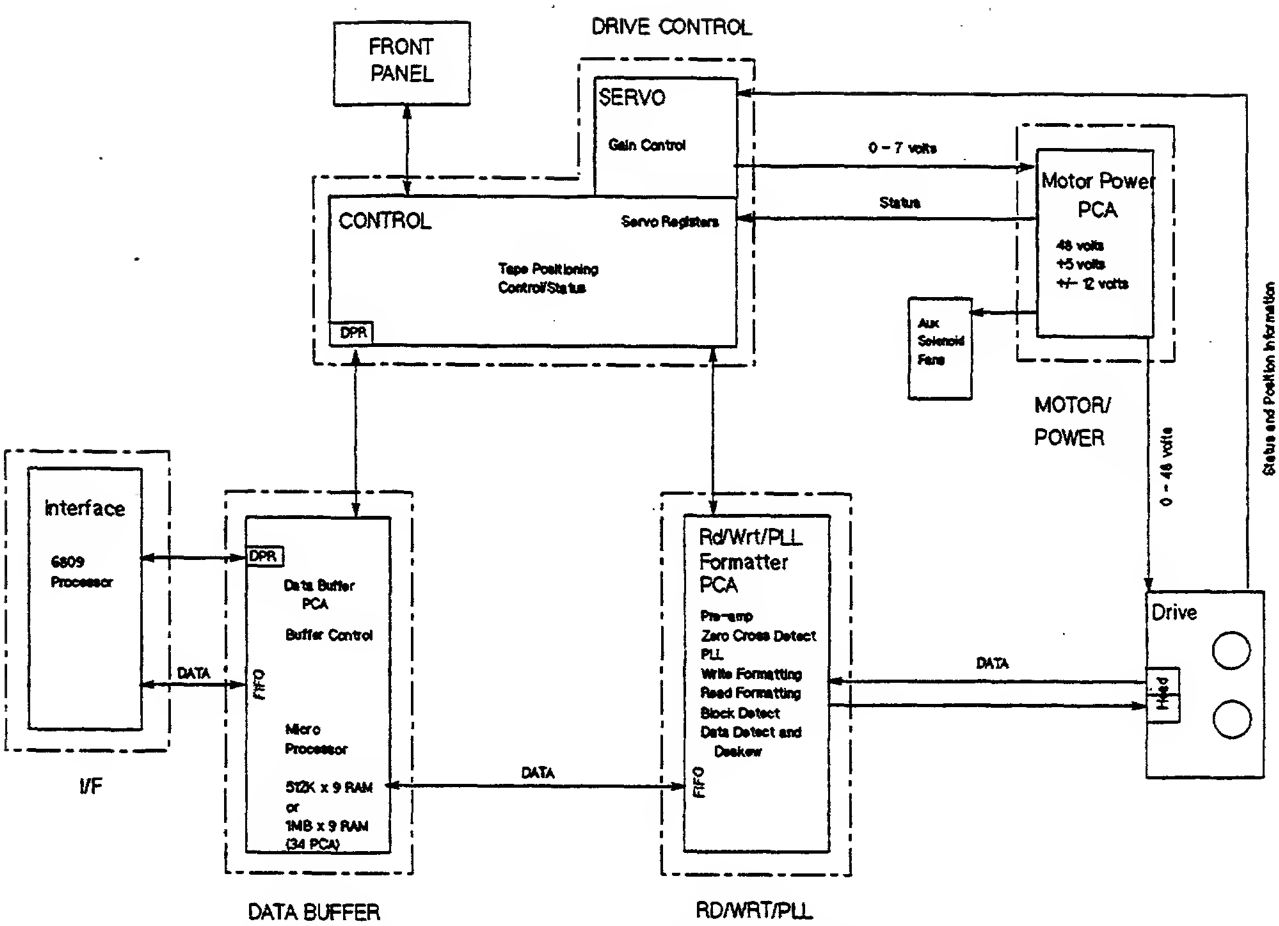
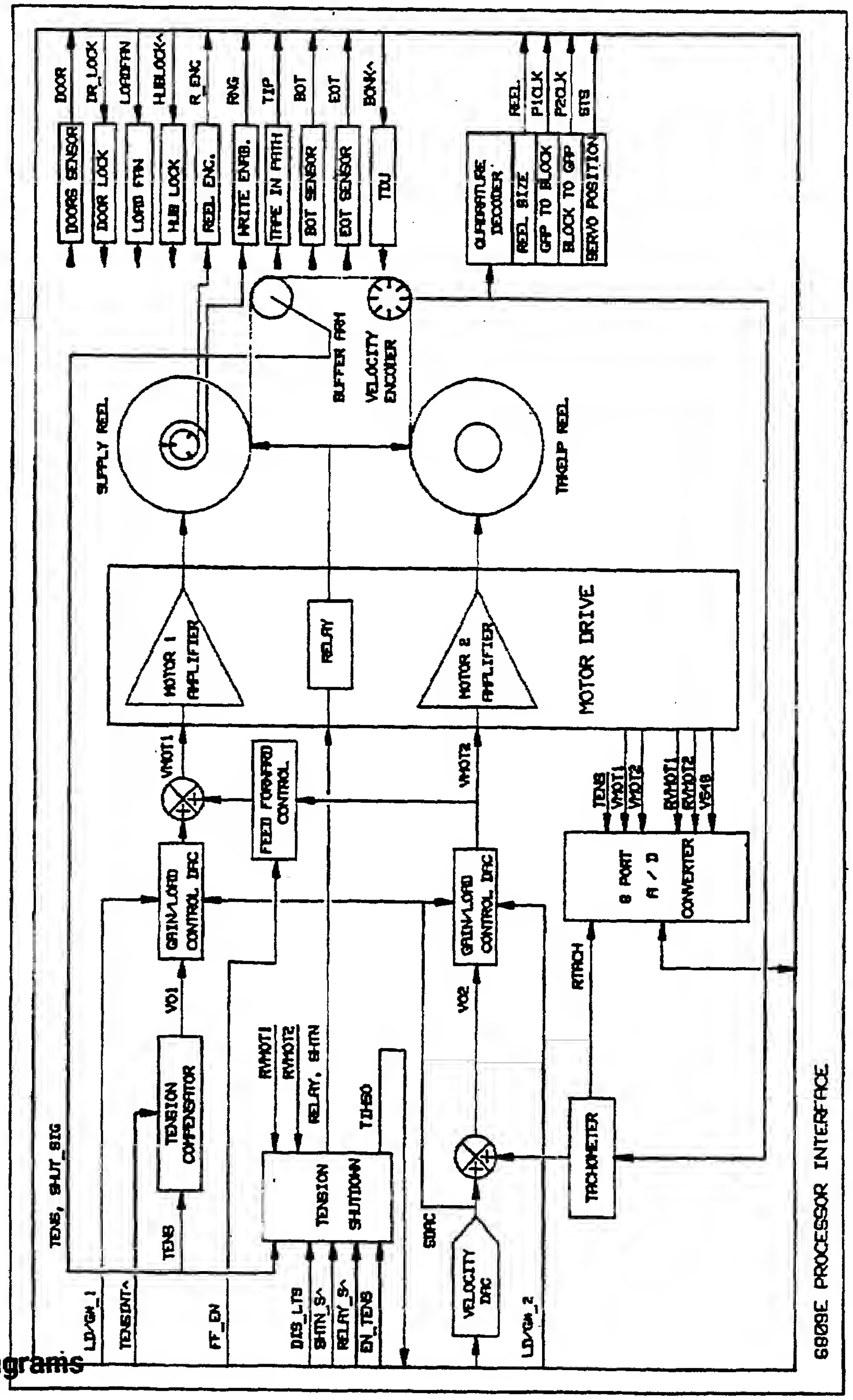


Figure 12-2. Overall Block Diagram (3-PCA Version)

Servo Controller Block Diagram



Power Distribution Block Diagrams

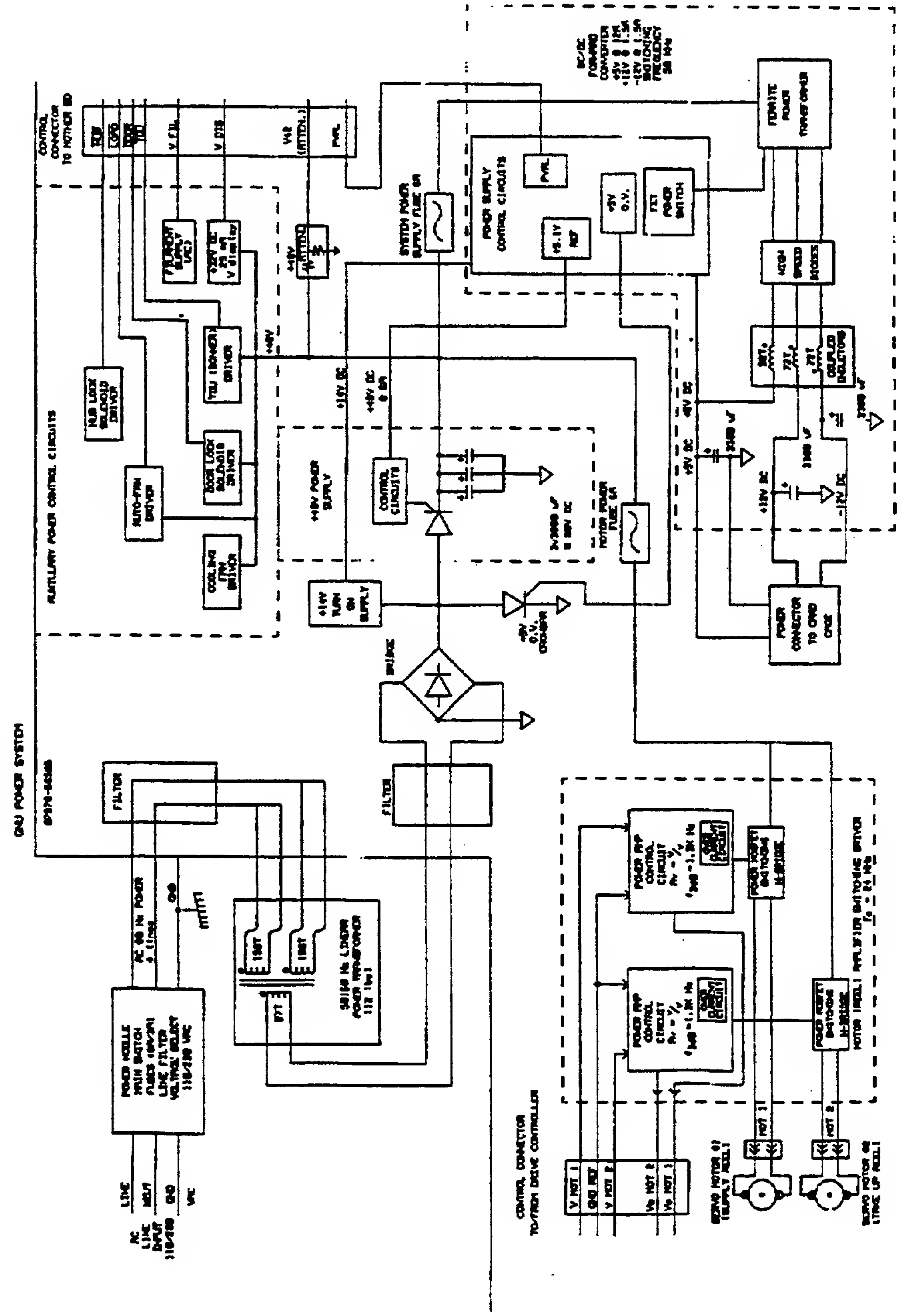


Figure 12-4. Power Distribution Block Diagram (-6xx05)

Motherboard PCA

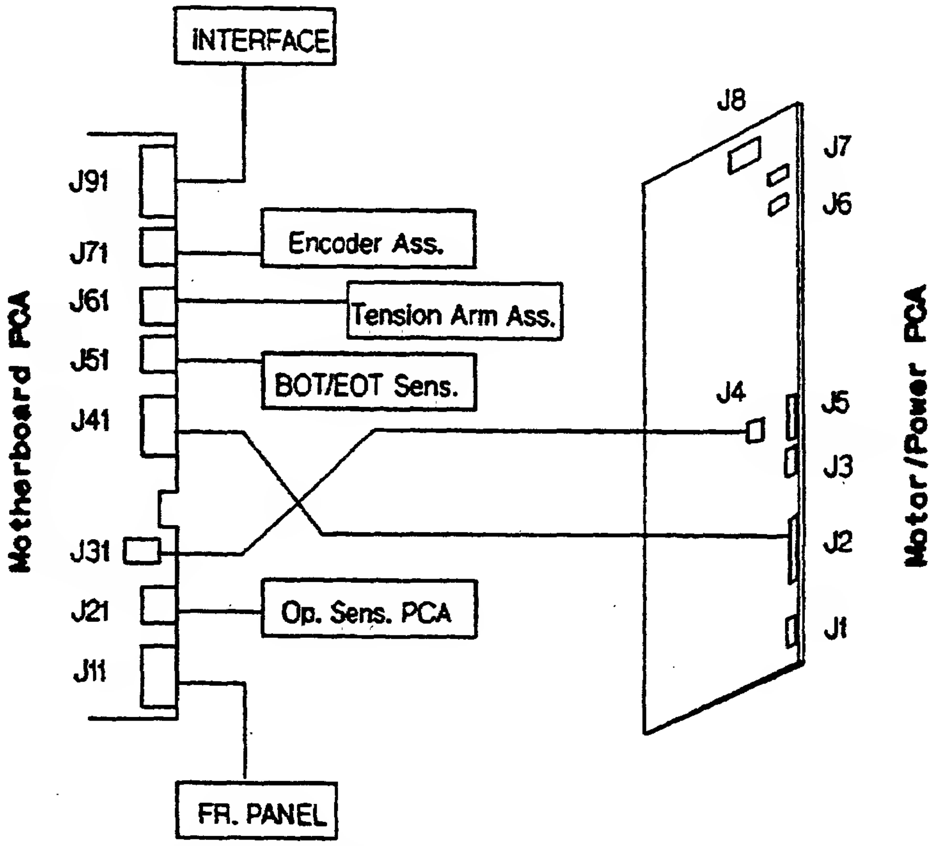


Figure 12-5. Motherboard PCA External Cabling (with -6xx05 Motor/Power PCA)

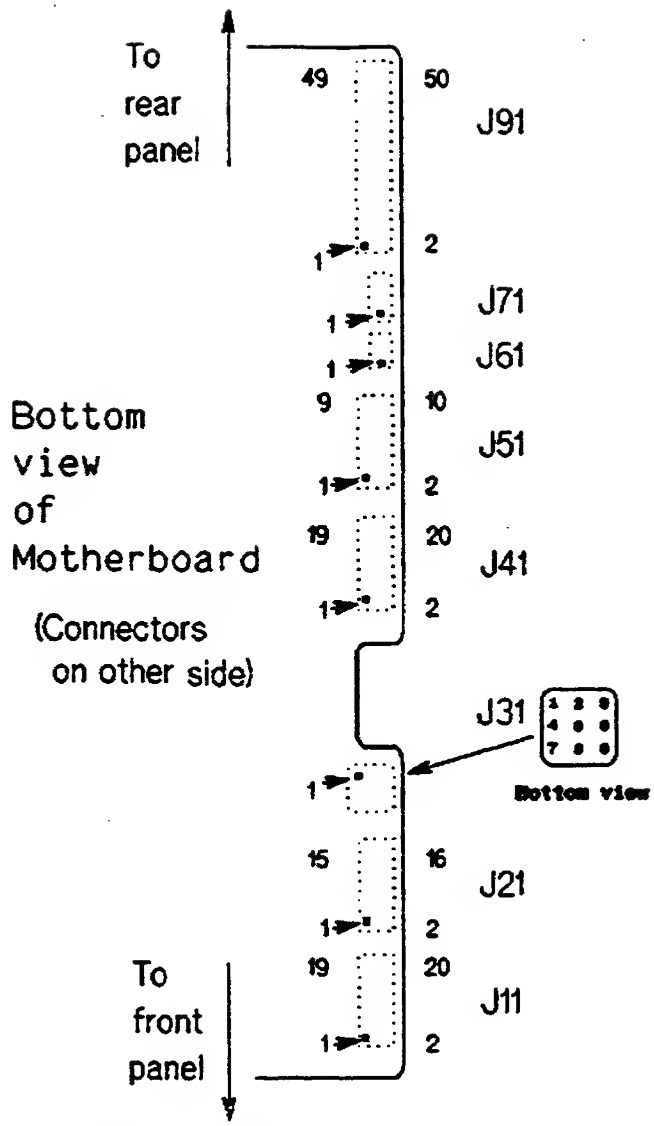


Figure 12-6. Motherboard PCA External Connector Pin Positiions

Table 12-1. Motherboard PCA Connectors

Number	Description
J11	Front Panel
J21	Op-Sens
J31	Power
J41	Motor Drive
J51	BOT/EOT
J61	Tension
J71	Speed Encoder
J91	Interface

J11 Front Panel

J11 Front Panel (20-pin ribbon)

Pin Number	Signal, etc.	Connects to Front Panel J1
Pin 1	+5V	Pin for Pin
Pin 2	SW 1 (OPTION)	Pin for Pin
Pin 3	SW 5 (ONLINE)	Pin for Pin
Pin 4	SW 2 (PREV)	Pin for Pin
Pin 5	SW 6 REWIND (7979A, 7980A, 7980XC) UNLOAD/REWIND (88780A/B)	Pin for Pin
Pin 6	SW 3 (NEXT)	Pin for Pin
Pin 7	GND	Pin for Pin
Pin 8	SW 4 (ENTER)	Pin for Pin
Pin 9	GND	Pin for Pin
Pin 10	FILAMENT 2	Pin for Pin
Pin 11	SW 7 (RESET)	Pin for Pin
Pin 12	FILAMENT 1	Pin for Pin
Pin 13	Not Used	
Pin 14	+31 VDC	Pin for Pin
Pin 15	SW 8 UNLOAD (7979A, 7980A, 7980XC) DENSITY (88780A/B)	Pin for Pin
Pin 16	SCLK	Pin for Pin
Pin 17	GND	Pin for Pin
Pin 18	SDATA	Pin for Pin
Pin 19	DSTROBE	Pin for Pin
Pin 20	BLANK DISPLAY	Pin for Pin

J21 Op-Sens (16-pin ribbon)

Pin Number	Signal	Connects to Sensor PCA J2
Pin 1	DOOR_LED+	Pin for Pin
Pin 2	DOOR_LED-	Pin for Pin
Pin 3	DOOR_VCC	Pin for Pin
Pin 4	DOOR_SIG	Pin for Pin
Pin 5	RW_LED+	Pin for Pin
Pin 6	RENC_LED-	Pin for Pin
Pin 7	RW_VCC	Pin for Pin
Pin 8	RENC_SIG	Pin for Pin
Pin 9	WREN_LED-	Pin for Pin
Pin 10	WREN_SIG	Pin for Pin
Pin 11	TIP_LED+	Pin for Pin
Pin 12	TIP_LED-	Pin for Pin
Pin 13	TIP_COLL	Pin for Pin
Pin 14	TIP_SIG	Pin for Pin
Pin 15	GND4	Pin for Pin
Pin 16	OPT_CON	Pin for Pin

J31 Power (9-pin MOLEX™)

Pin Number	Signal, etc.	Color	Connects To
Pin 1	+12V	Green	Motor/Power PCA J4(1)
Pin 2	GND	White	Motor/Power PCA J4(2)
Pin 3	+5V	Red	Motor/Power PCA J4(3)
Pin 4	-12V	Blue	Motor/Power PCA J4(4)
Pin 5	GND	White	Motor/Power PCA J4(5)
Pin 6	+5V	Red	Motor/Power PCA J4(6)
Pin 7	GND	Green	Casting (Main Power Switch mounting screw)
Pin 8	GND	White	-HPIB Intf. J2(2) -SCSI Sngl-End Intf. J4(2) -SCSI Diff. Intf. J4(2) -Pertec-comp. Intf. P4(2)
Pin 9	+5V	Red	-HPIB Intf. J2(1) -SCSI Sngl-End Intf. J4(1) -SCSI Diff. Intf. J4(1) -Pertec-comp. Intf. P4(1)

J41 -Motor Drive (20-pin ribbon)

Pin Number	Signal, etc.	Connects To Motor/Power PCA J2
Pin 1	SHTN	Pin for Pin
Pin 2	RELAY*	Pin for Pin
Pin 3	PVALID	Pin for Pin
Pin 4	DOOR LOCK*	Pin for Pin
Pin 5	LOAD FAN*	Pin for Pin
Pin 6	HUB LOCK*	Pin for Pin
Pin 7	SYSGROUND	Pin for Pin
Pin 8	BONKER* (TDU)	Pin for Pin
Pin 9	GND	Pin for Pin
Pin 10	+10V DISPLAY FILAMENT (FIL2)	Pin for Pin
Pin 11	Vs48(returned, divided 48V)	Pin for Pin
Pin 12	+5V DISPLAY FILAMENT (FIL1)	Pin for Pin
Pin 13	Not used	
Pin 14	30V FLUORESCENT DISPLAY	Pin for Pin
Pin 15	GND	Pin for Pin
Pin 16	RETURNED TAKEUP MOTOR VOLTAGE	Pin for Pin
Pin 17	INPUT TAKEUP MOTOR VOLTAGE	Pin for Pin
Pin 18	RETURNED SUPPLY MOTOR VOLTAGE	Pin for Pin
Pin 19	INPUT SUPPLY MOTOR VOLTAGE	Pin for Pin
Pin 20	+5V	Pin for Pin

J51 - BOT/EOT (10-pin ribbon)

Pin Number	Signal, etc.	Connects To BOT/EOT Sensor (direct connect)
Pin 1	SHUT_LED-	Pin for Pin
Pin 2	SHUT_SIG	Pin for Pin
Pin 3	EBS_EMM	Pin for Pin
Pin 4	EOT_COLL	Pin for Pin
Pin 5	EOT_LED-	Pin for Pin
Pin 6	BOT_COLL	Pin for Pin
Pin 7	BOT_LED-	Pin for Pin
Pin 8	EBS_LED+	Pin for Pin
Pin 9	GND2	Pin for Pin
Pin 10	TEN_CON	Pin for Pin

J61 - Tension (3-pin ribbon)

Pin Number	Signal, etc.	Connects To Tension Sensor Assembly (direct connect)
Pin 1	VR4+	Pin for Pin
Pin 2	TEN_SIG	Pin for Pin
Pin 3	VR4-	Pin for Pin

J71 - Speed Encoder (5-pin clip)

Pin Number	Signal, etc.	Color	Connects to Speed Encoder Assembly
Pin 1	GND1	Green	Pin for Pin
Pin 2	SPD_CON	Purple	Pin for Pin
Pin 3	PH_A	Orange	Pin for Pin
Pin 4	+5V	Blue	Pin for Pin
Pin 5	PH_B	Black	Pin for Pin

J91 - Interface (50-pin ribbon)

Pin Number	Signal, etc.	Connects to Interface
Pin 1	GND	Pin for Pin[1]
Pin 2	IF_CON (GND)	Pin for Pin
Pin 3	GND	Pin for Pin
Pin 4	IF_HIGH	Pin for Pin
Pin 5	IA[9]	Pin for Pin
Pin 6	IA[8]	Pin for Pin
Pin 7	IAD[7]	Pin for Pin
Pin 8	IAD[6]	Pin for Pin
Pin 9	IAD[5]	Pin for Pin
Pin 10	IAD[4]	Pin for Pin
Pin 11	IAD[3]	Pin for Pin
Pin 12	IAD[2]	Pin for Pin
Pin 13	IAD[1]	Pin for Pin
Pin 14	IAD[0]	Pin for Pin
Pin 15	ISEL*[2]	Pin for Pin
Pin 16	GND	Pin for Pin
Pin 17	SYSRESET	Pin for Pin
Pin 18	GND	Pin for Pin
Pin 19	IR/W*[2]	Pin for Pin
Pin 20	GND	Pin for Pin
Pin 21	IM/S*[2]	Pin for Pin
Pin 22	GND	Pin for Pin
Pin 23	IINTA	Pin for Pin
Pin 24	GND	Pin for Pin
Pin 25	IADS	Pin for Pin

1 J1 = HPIB; J2 = SCSI Single-Ended; J3 = SCSI Differential; P3 = Pertec-compatible

2 * Active Low

J91 - Interface (50-pin ribbon) (continued)

Pin Number	Signal, etc.	Connects to Interface
Pin 26	GND	Pin for Pin
Pin 27	ID/A*3	Pin for Pin
Pin 28	GND	Pin for Pin
Pin 29	GND	Pin for Pin
Pin 30	GNDS1	Pin for Pin
Pin 31	IWS*1	Pin for Pin
Pin 32	GND	Pin for Pin
Pin 33	IWRGA	Pin for Pin
Pin 34	GND	Pin for Pin
Pin 35	IRSA	Pin for Pin
Pin 36	GND	Pin for Pin
Pin 37	IRRQ*1	Pin for Pin
Pin 38	GND	Pin for Pin
Pin 39	IEOD	Pin for Pin
Pin 40	IPAR	Pin for Pin
Pin 41	ID[7]	Pin for Pin
Pin 42	ID[6]	Pin for Pin
Pin 43	ID[5]	Pin for Pin
Pin 44	ID[4]	Pin for Pin
Pin 45	ID[3]	Pin for Pin
Pin 46	ID[2]	Pin for Pin
Pin 47	ID[1]	Pin for Pin
Pin 48	ID[0]	Pin for Pin
Pin 49	GND	Pin for Pin
Pin 50	GND	Pin for Pin

1 * Active Low

Motor/Power PCA

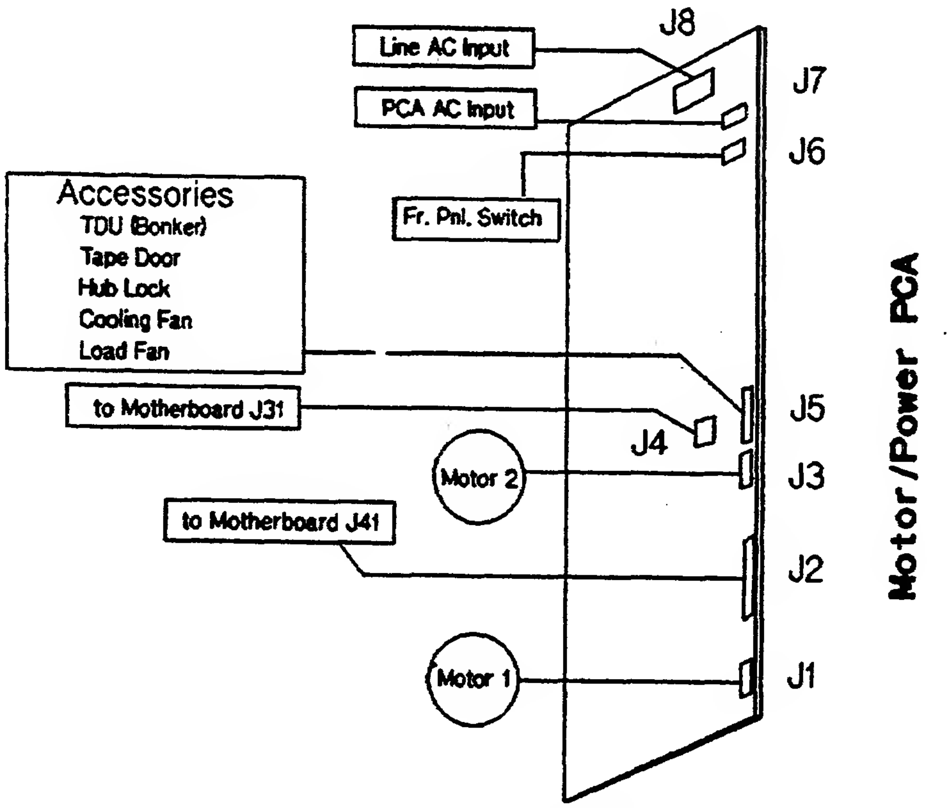


Figure 12-7. Motor/Power External Cabling (07980-6xx05, 88780-6xx05)

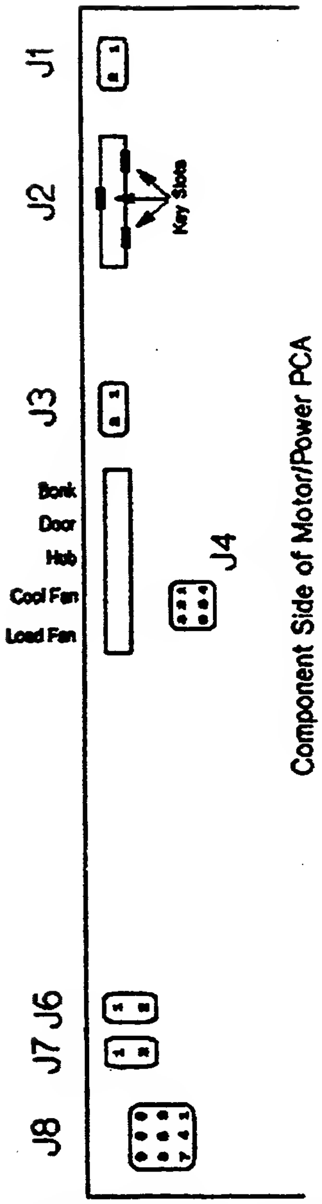


Figure 12-8. Motor/Power Pin Positions (07980-6xx05, 88780,6xx05)

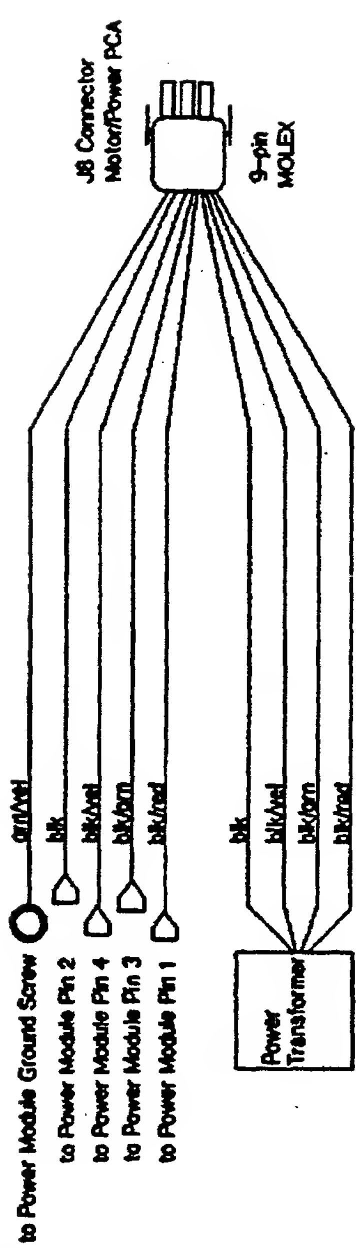


Figure 12-9. Power Cable to 07980-6xx05 and 88780-6xx05 PCA

07980-6xx05 and 88780-6xx05

Connectors	Description
J1	Supply Motor
J2	To Motherboard
J3	Takeup Motor
J4	System Power Supply
J5	Accessories Drive
J6	Front Panel Switch Power
J7	Motor/Power PCA AC Input
J8	Line AC Input

J1 - Supply Motor (2-pin MOLEX™)

Pin Number	Signal, etc.	Color	Connects to Supply Motor (direct connect)
Pin 1	Neutral	Black	Pin for Pin
Pin 2	Hot	Red	Pin for Pin

J2 - Interface to Motherboard (20-pin ribbon)

Pin Number	Signal, etc.	Connects to Motherboard J41
Pin 1	SHTN	Pin for Pin
Pin 2	RELAY*[1]	Pin for Pin
Pin 3	PVALID	Pin for Pin
Pin 4	DOOR LOCK*	Pin for Pin
Pin 5	LOAD FAN*	Pin for Pin
Pin 6	HUB LOCK*	Pin for Pin
Pin 7	SYSGROUND	Pin for Pin
Pin 8	BONKER* (TDU)	Pin for Pin
Pin 9	GND	Pin for Pin
Pin 10	+10V DISPLAY FILAMENT (FIL2)	Pin for Pin
Pin 11	Vs48(returned, divided 48V)	Pin for Pin
Pin 12	+5V DISPLAY FILAMENT (FIL1)	Pin for Pin
Pin 13	Not used	
Pin 14	30V FLUORESCENT DISPLAY	Pin for Pin
Pin 15	GND	Pin for Pin
Pin 16	RETURNED TAKEUP MOTOR VOLTAGE	Pin for Pin
Pin 17	INPUT TAKEUP MOTOR VOLTAGE	Pin for Pin
Pin 18	RETURNED SUPPLY MOTOR VOLTAGE	Pin for Pin
Pin 19	INPUT SUPPLY MOTOR VOLTAGE	Pin for Pin
Pin 20	+5V	Pin for Pin

1 * is active low

J3 - Takeup Motor (2-pin MOLEX™)

Pin Number	Signal,etc.	Color	Connects to Takeup Motor (direct connect)
Pin 1	Neutral	Black	Pin for Pin
Pin 2	Hot	Red	Pin for Pin

J4 - System Power Supply (6-pin MOLEX™)

Pin Number	Signal,etc.	Color	Connects to Motherboard PCA J31
Pin 1	+12V	Green	Pin for Pin
Pin 2	-12V	White	Pin for Pin
Pin 3	GND	Red	Pin for Pin
Pin 4	GND	Blue	Pin for Pin
Pin 5	+5V	White	Pin for Pin
Pin 6	+5V	Red	Pin for Pin
Pin 7,8,9	Not Used		

J5 - Accessories Drive (15-post Bergstrip™)

Pin Number	Signal,etc.	Color	Connects To
Pin 1	BONKER (TDU)	Black	TDU 24V Solenoid
Pin 2	BONKER	Brown	"
Pin 3	Not used		
Pin 4	DOOR	Black	Door 24V Solenoid
Pin 5	DOOR	Yellow	"
Pin 6	Not used		
Pin 7	HUB LOCK	Black	Hub Lock Solenoid
Pin 8	HUB LOCK	Green	"
Pin 9	Not used		
Pin 10	COOLING FAN	Black	Clip - then cooling fan
Pin 11	COOLING FAN	Red	"
Pin 12	Not used		
Pin 13	LOAD FAN	Black	Clip - then load fan
Pin 14	LOAD FAN	Purple	"
Pin 15	Not used		

J6 - Front Panel Switch Power (2-pin MOLEX™)

Pin Number	Signal,etc.	Color	Connects To
Pin 1	Line Out/Open	Blue	Front Panel Power Switch
Pin 2	Line In	White	Front Panel Power Switch

J7 - Motor/Power PCA AC Input (2-pin MOLEX™)

Pin Number	Signal,etc.	Color	Connects To
Pin 1	Main Power	Brown	Transformer Secondary
Pin 2	Main Power	Brown	Transformer Secondary

J8 - Line AC Input (9-pin MOLEX™)

Pin Number	Signal,etc.	Color	Connects To
Pin 1	Hot	Black/Red	Power Module (Figure 12-14)
Pin 2	Hot	Black/Red	Linear Power Transformer
Pin 3	Earth GND	Green/Yellow	Power Module (Figure 12-14)
Pin 4	Line Select/ Neutral	Black/Green	Power Module (Figure 12-14)
Pin 5	"	Black/Green	Linear Power Transformer
Pin 6	Line Select/Hot	Black/Yellow	Power Module (Figure 12-14)
Pin 7	Neutral	Black	Power Module (Figure 12-14)
Pin 8	Neutral	Black	Linear Power Transformer
Pin 9	Line Select/Hot	Black/Yellow	Linear Power Transformer

Power Module

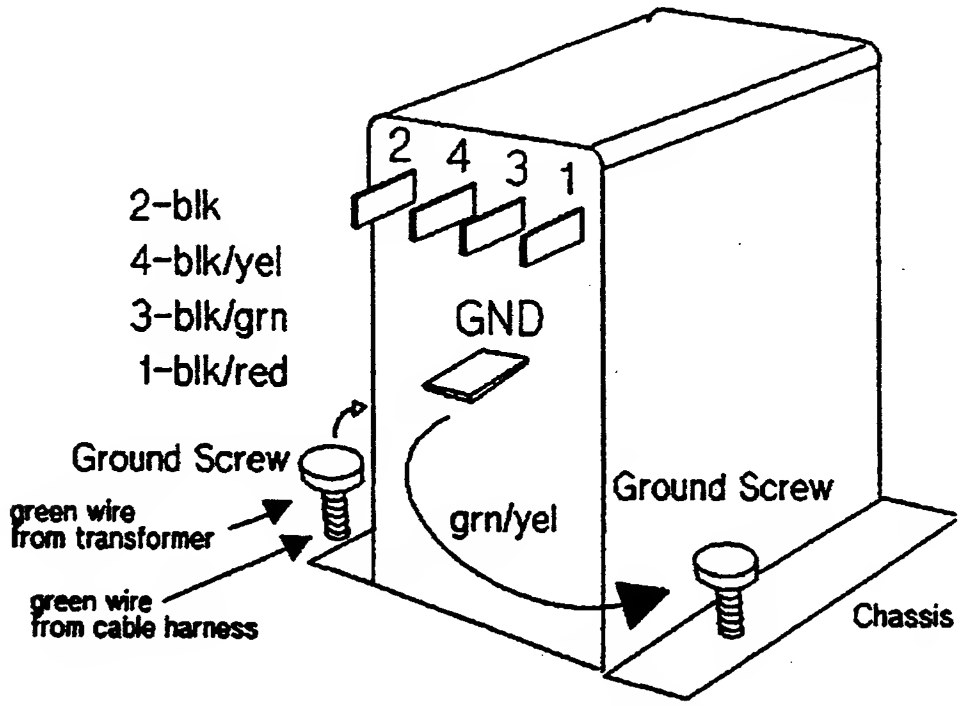


Figure 12-10. Rear Panel Power Module (07980-67919)

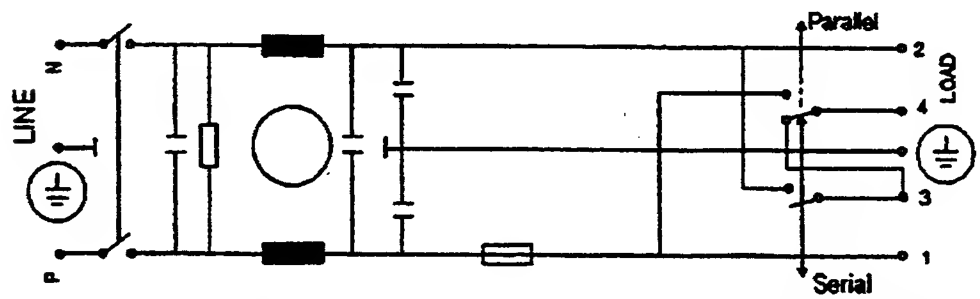


Figure 12-11. Rear Panel Power Module Schematic/Pinout

Wiring Harness

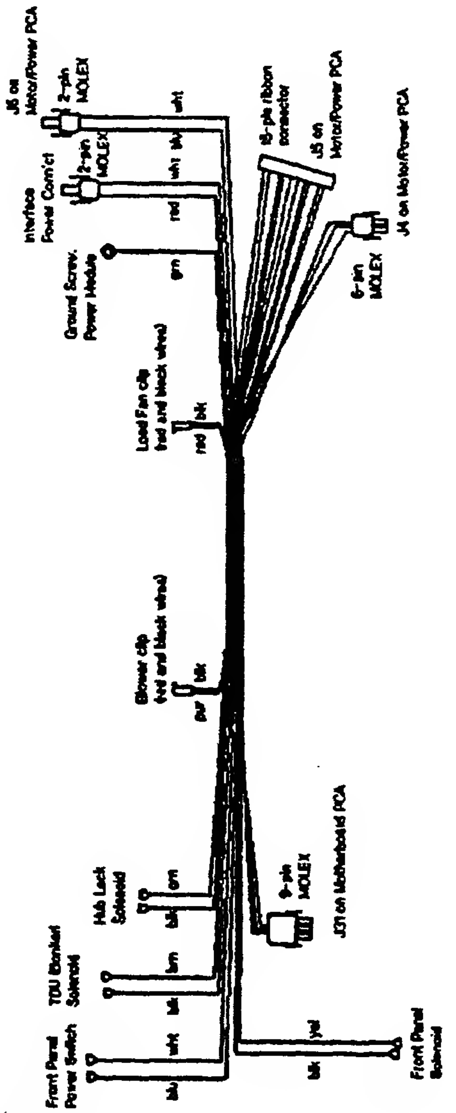


Figure 12-12. Wiring Harness (07980-60070)

Sensor PCA

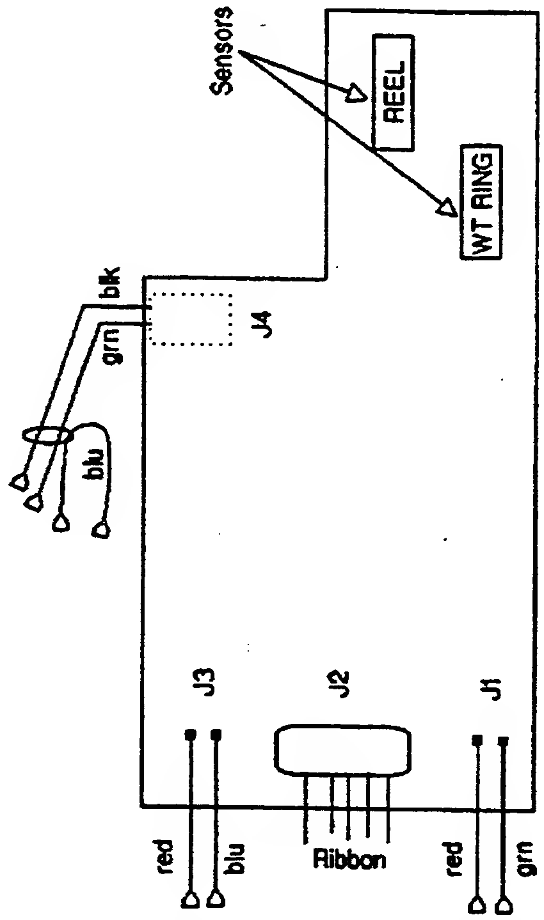


Figure 12-13. Sensor PCA Cabling

Sensor PCA
(Drawing on preceding page)

07980-6xx09

Connectors

Number	Description
J1	To tape-in-path LED detector
J2	Interface
J3	To tape-in-path LED
J4	To front panel microswitches

J1 - To tape-in-path LED detector (2 direct-connect wires)

Pin Number	Signal, etc.	Color	Connects to tape-in-path detector
Pin 1	TIP_LED-	Blue	Pin for Pin
Pin 2	TIP_LED+	Red	Pin for Pin

J2 -Interface (16-pin RIBBON)

Pin Number	Signal, etc.	Connects to Motherboard PCA J21
Pin 1	DOOR_LED+	Pin for Pin
Pin 2	DOOR_LED-	Pin for Pin
Pin 3	DOOR_COLL	Pin for Pin
Pin 4	DOOR-SIG	Pin for Pin
Pin 5	RW_LED+	Pin for Pin
Pin 6	RENC_LED-	Pin for Pin
Pin 7	RW_COLL	Pin for Pin
Pin 8	RENC_SIG	Pin for Pin
Pin 9	WREN_LED-	Pin for Pin
Pin 10	WREN_SIG	Pin for Pin
Pin 11	TIP_LED+	Pin for Pin
Pin 12	TIP_LED-	Pin for Pin
Pin 13	TIP_COLL	Pin for Pin
Pin 14	TIP_SIG	Pin for Pin
Pin 15	GND4	Pin for Pin
Pin 16	OPT_CON	Pin for Pin

J3 - to tape-in-path LED (2 direct-connect wires)

Pin Number	Signal, etc.	Color	Connects to tape-in-path LED
Pin 1	TIP_LED-	Blue	Pin for Pin
Pin 2	TIP_LED+	Red	Pin for Pin

J4 - to front panel microswitches (2 direct-connect wires)

Pin Number	Signal, etc.	Color	Connects To
Pin 1	GND	Black	front panel "tape door open/closed" microswitch
Pin 2	OUT	Green	front panel "top cover open/closed" microswitch
Pin 3	VCC		Not used, open hole
Pin 4	LED-		Not used, open hole
Pin 5	VCC		Not used, open hole

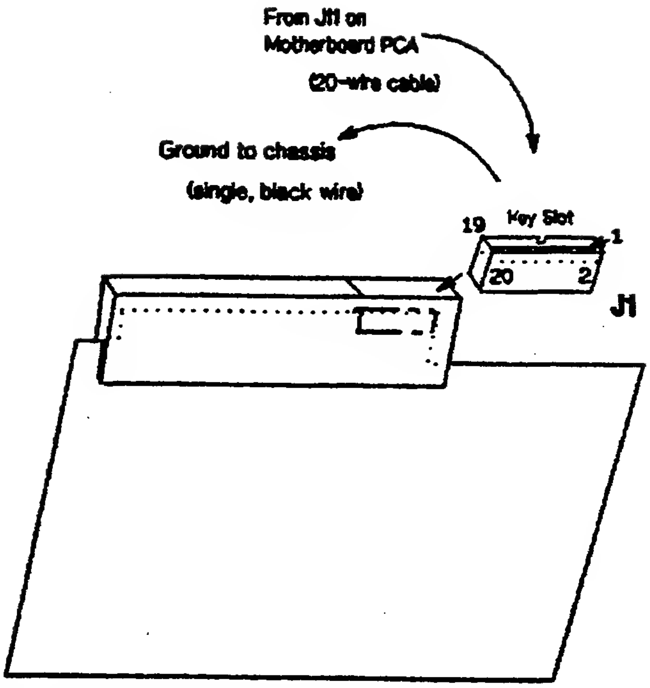


Figure 12-14. Front Panel Display Connector Pins

Front Panel PCA

07980-6xx08

Connectors

Number	Description
J1	Motherboard to Front Panel

J1 -Front Panel (20-pin RIBBON)

Pin Number	Signal, etc.	Connects to Motherboard PCA J11
Pin 1	VCC	Pin for Pin
Pin 2	SW 1 (OPTION)	Pin for Pin
Pin 3	SW 5 (ONLINE)	Pin for Pin
Pin 4	SW 2 (PREV)	Pin for Pin
Pin 5	SW 6	Pin for Pin
	REWIND (7979A, 7980A, 7980XC)	
	UNLOAD/REWIND (88780A)	
Pin 6	SW 3 (NEXT)	Pin for Pin
Pin 7	GND	Pin for Pin
Pin 8	SW 4 (ENTER)	Pin for Pin
Pin 9	GND	Pin for Pin
Pin 10	FILAMENT 2	Pin for Pin
Pin 11	SW 7 (RESET)	Pin for Pin
Pin 12	FILAMENT 1	Pin for Pin
Pin 13	Not used	Pin for Pin
Pin 14	+31 VDC	Pin for Pin
Pin 15	SW 8	Pin for Pin
	UNLOAD (7979A, 7980A, 7980XC)	
	DENSITY (88780A)	
Pin 16	SCLK	Pin for Pin
Pin 17	GND	Pin for Pin
Pin 18	SDATA	Pin for Pin
Pin 19	DSTROBE	Pin for Pin
Pin 20	BLANK DISPLAY	Pin for Pin
	Foil Shield grounding cable	Chassis

Read/Write//PLL PCA

07980-6xx01

Read/Write/Formatter/PLL PCA

07980-6xx21 and 88780-6xx21

07980-6xx31

Connectors

Number	Description
J1	From write head
J2	From read head

J1 - to Write Head (26-pin RIBBON)

Pin Number	Signal, etc.	Connects to Write Head
Pin 1	ERASE_LO	Pin for Pin
Pin 2	ERASE_HI	Pin for Pin
Pin 3	CHANNEL 1	Pin for Pin
Pin 4	"	Pin for Pin
Pin 5	CHANNEL 2	Pin for Pin
Pin 6	"	Pin for Pin
Pin 7	CHANNEL 3	Pin for Pin
Pin 8	"	Pin for Pin
Pin 9	CHANNEL 4	Pin for Pin
Pin 10	"	Pin for Pin
Pin 11	CHANNEL 5	Pin for Pin
Pin 12	"	Pin for Pin
Pin 13	WRITE CURRENT	Pin for Pin
Pin 14	"	Pin for Pin
Pin 15	CHANNEL 6	Pin for Pin
Pin 16	"	Pin for Pin
Pin 17	CHANNEL 7	Pin for Pin
Pin 18	"	Pin for Pin
Pin 19	CHANNEL 8	Pin for Pin
Pin 20	"	Pin for Pin
Pin 21	CHANNEL 9	Pin for Pin
Pin 22	"	Pin for Pin
Pin 23	Not used	
Pin 24	Not used	
Pin 25	GND	Pin for Pin
Pin 26	GND	Pin for Pin

J2 - to Read Head (26-pin RIBBON)

Pin Number	Signal, etc.	Connects to Read Head
Pin 1	GND	Pin for Pin
Pin 2	GND	Pin for Pin
Pin 3	GND	Pin for Pin
Pin 4	GND	Pin for Pin
Pin 5	GND	Pin for Pin
Pin 6	GND	Pin for Pin
Pin 7	READ CHANNEL 1	Pin for Pin
Pin 8	"	Pin for Pin
Pin 9	READ CHANNEL 2	Pin for Pin
Pin 10	"	Pin for Pin
Pin 11	READ CHANNEL 3	Pin for Pin
Pin 12	"	Pin for Pin
Pin 13	READ CHANNEL 4	Pin for Pin
Pin 14	"	Pin for Pin
Pin 15	READ CHANNEL 5	Pin for Pin
Pin 16	"	Pin for Pin
Pin 17	GND	Pin for Pin
Pin 18	GND	Pin for Pin
Pin 19	READ CHANNEL 6	Pin for Pin
Pin 20	"	Pin for Pin
Pin 21	READ CHANNEL 7	Pin for Pin
Pin 22	"	Pin for Pin
Pin 23	READ CHANNEL 8	Pin for Pin
Pin 24	"	Pin for Pin
Pin 25	READ CHANNEL 9	Pin for Pin
Pin 26	"	Pin for Pin

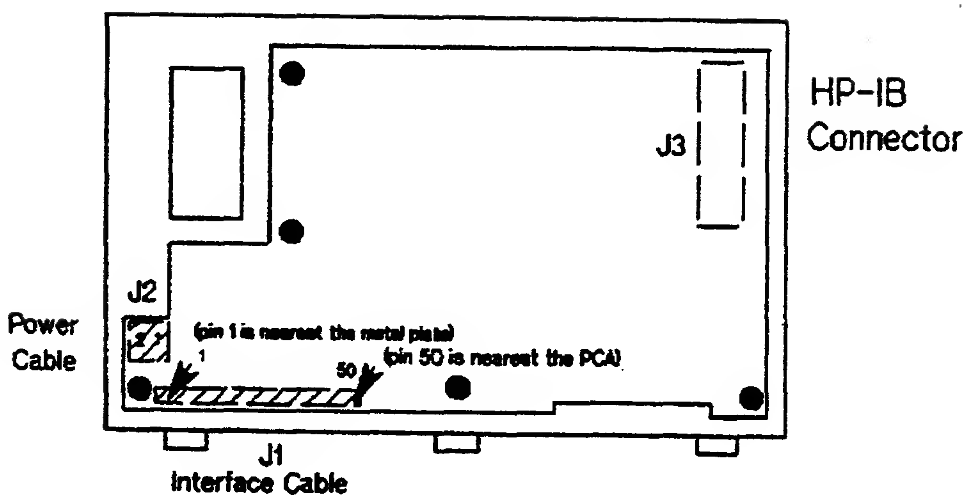


Figure 12-15.
HP-IB Interface Pin Positions
(PCA shown mounted)

HP-IB Interface PCA

07980-6xx07

Connectors

Number	Description
J1	Interface cable to Motherboard
J2	Power from Motherboard
J3	HP-IB Connector

J1 - Interface-to-Motherboard (50-pin RIBBON)

Pin Number	Signal, etc.	Connects to Motherboard PCA J91
Pin 1	GND	Pin for Pin
Pin 2	IF_CON (GND)	Pin for Pin
Pin 3	GND	Pin for Pin
Pin 4	IF_HIGH	Pin for Pin
Pin 5	IA[9]	Pin for Pin
Pin 6	IA[8]	Pin for Pin
Pin 7	IAD[7]	Pin for Pin
Pin 8	IAD[6]	Pin for Pin
Pin 9	IAD[5]	Pin for Pin
Pin 10	IAD[4]	Pin for Pin
Pin 11	IAD[3]	Pin for Pin
Pin 12	IAD[2]	Pin for Pin
Pin 13	IAD[1]	Pin for Pin
Pin 14	IAD[0]	Pin for Pin
Pin 15	ISEL*	Pin for Pin
Pin 16	GND	Pin for Pin
Pin 17	SYSRESET	Pin for Pin
Pin 18	GND	Pin for Pin
Pin 19	IR/W*	Pin for Pin
Pin 20	GND	Pin for Pin
Pin 21	IM/S*	Pin for Pin
Pin 22	GND	Pin for Pin
Pin 23	IINTA	Pin for Pin
Pin 24	GND	Pin for Pin
Pin 25	IADS	Pin for Pin

J1 - Interface-to-Motherboard (50-pin RIBBON) (continued)

Pin Number	Signal, etc.	Connects to Motherboard PCA J91
Pin 26	GND	Pin for Pin
Pin 27	ID/A*	Pin for Pin
Pin 28	GND	Pin for Pin
Pin 29	GND	Pin for Pin
Pin 30	GNDS1	Pin for Pin
Pin 31	IWS*	Pin for Pin
Pin 32	GND	Pin for Pin
Pin 33	IWRGA	Pin for Pin
Pin 34	GND	Pin for Pin
Pin 35	IRSA	Pin for Pin
Pin 36	GND	Pin for Pin
Pin 37	IRRQ*	Pin for Pin
Pin 38	GND	Pin for Pin
Pin 39	IEOD	Pin for Pin
Pin 40	IPAR	Pin for Pin
Pin 41	ID[7]	Pin for Pin
Pin 42	ID[6]	Pin for Pin
Pin 43	ID[5]	Pin for Pin
Pin 44	ID[4]	Pin for Pin
Pin 45	ID[3]	Pin for Pin
Pin 46	ID[2]	Pin for Pin
Pin 47	ID[1]	Pin for Pin
Pin 48	ID[0]	Pin for Pin
Pin 49	GND	Pin for Pin
Pin 50	GND	Pin for Pin

J2 -Power from Motherboard (2-pin MOLEX™)

Pin Number	Signal, etc.	Color	Connects to Motherboard PCA J31
Pin 1	+5 V	Red	J31(9)
Pin 2	GND	White	J31(8)

J3 - HP-IB Connector (24-pin)

Pin Number	Signal	Pin Number	Signal
Pin 1	DI/O 1	Pin 13	DI/O 5
Pin 2	DI/O 2	Pin 14	DI/O 6
Pin 3	DI/O 3	Pin 15	DI/O 7
Pin 4	DI/O 4	Pin 16	DI/O 8
Pin 5	EOI	Pin 17	REN
Pin 6	DAV	Pin 18	DAV GND
Pin 7	NRFD	Pin 19	NRFD GND
Pin 8	NDAC	Pin 20	NDAC GND
Pin 9	IFC	Pin 21	IFC GND
Pin 10	SRQ	Pin 22	SRQ GND
Pin 11	ATN	Pin 23	ATN GND
Pin 12	SHIELD	Pin 24	LOGIC GND

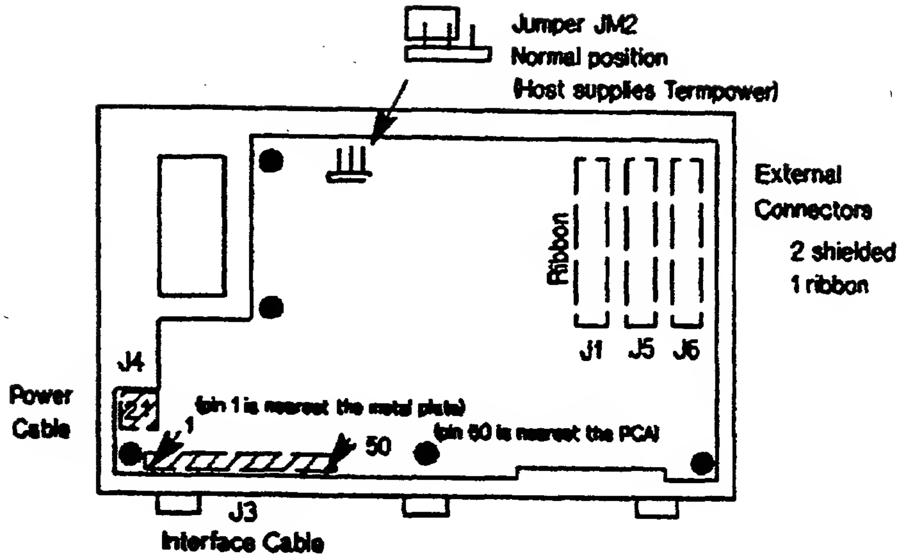


Figure 12-16.
Single-Ended SCSI Interface Pin Positions
(PCA shown mounted)

SCSI Single-Ended Interface PCA

88780-6xx15 and 88780-6xx35

Connectors

Number	Description
J1	Ribbon SCSI bus connector
J3	Interface cable to Motherboard
J4	Power from Motherboard
J5	Shielded SCSI bus connector
J6	Shielded SCSI bus connector
JM2	Termpower jumper

J1, J5, J6 -SCSI bus connector (50-pin RIBBON)

Pin Number	Signal	Pin Number	Signal
Pin 1	GND	Pin 26	Termpower (+5V)
Pin 2	-Data Bit 0	Pin 27	GND
Pin 3	GND	Pin 28	GND
Pin 4	-Data Bit 1	Pin 29	GND
Pin 5	GND	Pin 30	GND
Pin 6	-Data Bit 2	Pin 31	GND
Pin 7	GND	Pin 32	-ATN
Pin 8	-Data Bit 3	Pin 33	GND
Pin 9	GND	Pin 34	GND
Pin 10	-Data Bit 4	Pin 35	GND
Pin 11	GND	Pin 36	-BSY

J1, J5, J6 -SCSI bus connector (50-pin RIBBON) (continued)

Pin Number	Signal	Pin Number	Signal
Pin 12	-Data Bit 5	Pin 37	GND
Pin 13	GND	Pin 38	ACK
Pin 14	-Data Bit 6	Pin 39	GND
Pin 15	GND	Pin 40	-RST
Pin 16	-Data Bit 7	Pin 41	GND
Pin 17	GND	Pin 42	-MSG
Pin 18	-Data Bit P	Pin 43	GND
Pin 19	GND	Pin 44	-SEL
Pin 20	GND	Pin 45	GND
Pin 21	GND	Pin 46	-C/D
Pin 22	GND	Pin 47	GND
Pin 23	GND	Pin 48	-REQ
Pin 24	GND	Pin 49	GND
Pin 25	OPEN	Pin 50	-I/O

J3 - Interface to Motherboard (50-pin RIBBON)

See HPIB Interface PCA J1 description earlier in this section for signals going to tihs connector.

J4 - Power from Motherboard (2-pin MOLEX™)

Pin Number	Signal, etc.	Color	Connects to Motherboard PCA J31
Pin 1	+5 V	Red	J31(9)
Pin 2	GND	White	J31(8)

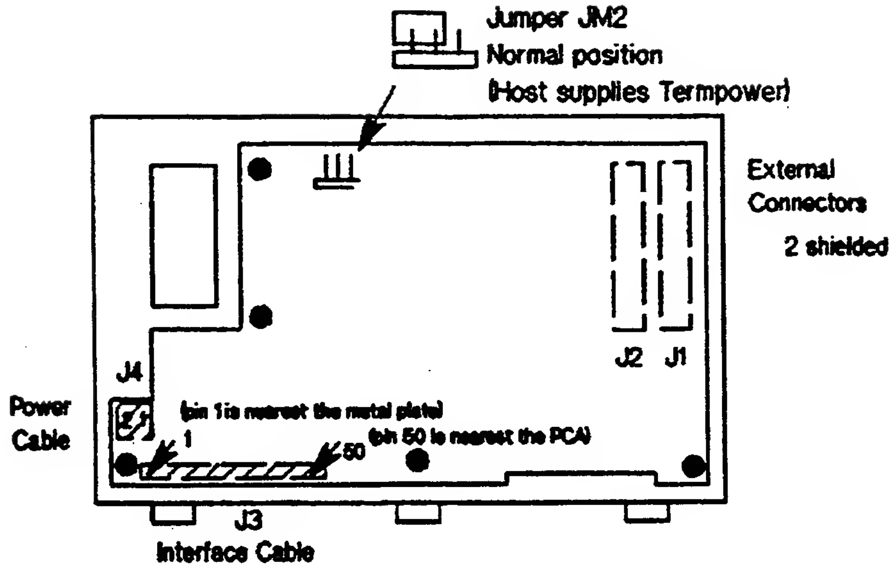


Figure 12-17.
Differential SCSI Interface Pin Positions
(PCA shown mounted)

SCSI Differential Interface PCA

88780-6xx16 or 88780-6xx36

Connectors

Number	Description
J1	Shielded SCSI bus connector
J2	Shielded SCSI bus connector
J3	Interface cable to Motherboard
J4	Power from Motherboard
JM2	Termpower jumper

J1, J2 - Shielded SCSI bus connectors (50-pin RIBBON)

Pin Number	Signal	Pin Number	Signal
Pin 1	SHIELD GND	Pin 26	TERMPWR (+5V)
Pin 2	GND	Pin 27	GND
Pin 3	+Data Bit 0	Pin 28	GND
Pin 4	-Data Bit 0	Pin 29	+ATN
Pin 5	+Data Bit 1	Pin 30	-ATN
Pin 6	-Data Bit 1	Pin 31	GND
Pin 7	+Data Bit 2	Pin 32	GND
Pin 8	-Data Bit 2	Pin 33	+BSY
Pin 9	+Data Bit 3	Pin 34	-BSY
Pin 10	-Data Bit 3	Pin 35	+ACK
Pin 11	+Data Bit 4	Pin 36	-ACK
Pin 12	-Data Bit 4	Pin 37	+RST

J1, J2 - Shielded SCSI bus connectors (50-pin RIBBON) (continued)

Pin Number	Signal	Pin Number	Signal
Pin 13	+Data Bit 5	Pin 38	-RST
Pin 14	-Data Bit 5	Pin 39	+MSG
Pin 15	+Data Bit 6	Pin 40	-MSG
Pin 16	-Data Bit 6	Pin 41	+SEL
Pin 17	+Data Bit 7	Pin 42	-SEL
Pin 18	-Data Bit 7	Pin 43	+C/D
Pin 19	+Data Bit P	Pin 44	-C/D
Pin 20	-Data Bit P	Pin 45	+REQ
Pin 21	DIFFSENS	Pin 46	-REQ
Pin 22	GND	Pin 47	+I/O
Pin 23	GND	Pin 48	-I/O
Pin 24	GND	Pin 49	GND
Pin 25	TERMPWR (+5V)	Pin 50	GND

J3 - Interface to Motherboard (50-pin RIBBON)

See HPIB Interface PCA J1 description earlier in this section for signals going to tihs connector.

J4 - Power from Motherboard (2-pin MOLEX™)

Pin Number	Signal, etc.	Color	Connects to Motherboard PCA J31
Pin 1	+5 V	Red	J31(9)
Pin 2	GND	White	J31(8)

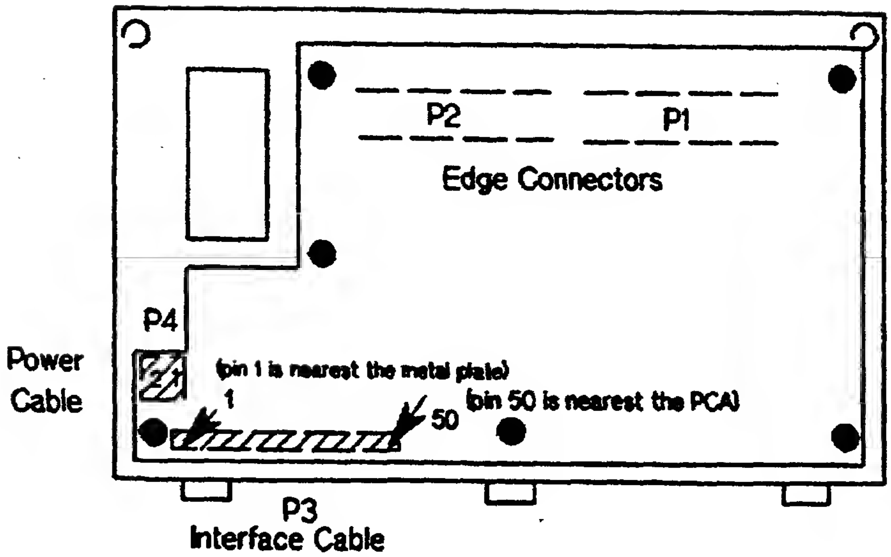


Figure 12-18.
Pertec-Compatible Interface Pin Positions
(PCA shown mounted)

Pertec-Compatible Interface PCA

88780-6xx22

Connectors

Number	Description
P1	Pertec-compatible connector
P2	Pertec-compatible connector
P3	Interface cable to Motherboard
P4	Power from Motherboard

For P1 and P2, bus definition and protocol are configurable for the following modes:

- CDC 92185-compatible mode
- CIPHER F880-compatible mode
- PERTEC FS1000-compatible mode

	88780A/B CIPHER	CIPH.	88780A/B CDC	PERTEC	
P1 Pin #					
14	n/a	n/a	n/a	n/a	SGL (unit check)
16	n/a	n/a	LOL	LOL	LOL (load/onl'n)
36	n/a	n/a	LGAP	LGAP(gap size)	RTH2 (3200/1600)
44	n/a	n/a	RTHR	RTHR(hi thresh)	RTH1 (gap size)
P2 Pin #					
24	OFL	REW/ UNL	OFL	OFL	OFL (offl/Rw/unl)
26	n/a	n/a	GCR	GCR	NRZ (diag ack)
40 | | n/a	n/a	HSPD	HSPD	SPEED (speed)	
50	n/a	n/a	HISP	HISP	DEN (25/100 ips)

Live Pin	Ground Pin	Signal Description	Signal Name
		P1 -Pertec-compatible connector (50-pin RIBBON)	
2	1	Formatter Busy	IFBY
4	3	Last Word	ILWD
6	5	Write Data 4	IW4
8	7	Initiate Command	IGO
10	9	Write Data 0	IWO
12	11	Write Data 1	IW1
14	13	(see preceding table)	definable
16	15	Load / Online	ILOL
18	17	Reverse	IREV
20	19	Rewind	IREW
22	21	Write Data Parity	IWP
24	23	Write Data 7	IW7
26	25	Write Data 3	IW3
28	27	Write Data 6	IW6
30	29	Write Data 2	IW2
32	31	Write Data 5	IW5
34	33	Write	IWRT
36	35	(see preceding table)	definable
38	37	Edit	IEDIT
40	39	Erase	IERASE
42	41	Write File Mark	IWFM
44	43	(see preceding table)	definable
46	45	Transport Address 0	ITAD0
48	47	Read Data 2	IR2
50	49	Read Data 3	IR3

Live Pin	Ground Pin	Signal Description	Signal Name
		P2 - Pertec-compatible connector (50-pin RIBBON)	
1	-	Read Data Parity	IRP
2	-	Read Data 0	IR0
3	-	Read Data 1	IR1
4	-	Load Point	ILDP
6	5	Read Data 4	IR4
8	7	Read Data 7	IR7
10	9	Read Data 6	IR6
12	11	Hard Error	IHER
14	13	File Mark	IFMK
16	15	Identification	IDENT
18	17	Formatter Enable	IFEN
20	19	Read Data 5	IR5
22	21	End of Tape	IEOT
24	23	Rewind/Unload	IRWU
26	25	(see preceding table)	definable
28	27	Ready	IRDY
30	29	Rewinding	IRWD
32	31	File Protect	IFPT
34	33	Read Strobe	IRSTR
36	35	Write Strobe	IWSTR
38	37	Data Busy	IDBY
40	39	(see preceding table)	definable
42	41	Corrected Error	ICER
44	43	Online	IONL
46	45	Transport Address 1	ITAD1
48	47	Formatter Address	IFAD
50	49	(see preceding table)	definable

P3 - Interface to Motherboard (50-pin RIBBON)

See HPIB Interface PCA J1 description earlier in this section for signals going to tihs connector.

P4 - Power from Motherboard (2-pin MOLEX™)

Pin Number	Signal, etc.	Color	Connects to Motherboard PCA J31
Pin 1	+5 V	Red	J31(9)
Pin 2	GND	White	J31(8)

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